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Design of High-Speed Low-Power ADCs for Wireless Communication

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ABSTRACT: With the explosive growth in wireless communication technologies, the demand for high-speed and low-power analog-to-digital converters (ADCs) has become more critical than ever. These ADCs are the backbone of modern transceivers, enabling accurate digitization of wideband signals while minimizing energy consumption. This paper presents a comprehensive study and design of a high-speed, low-power ADC tailored for next-generation wireless communication systems. Leveraging advanced CMOS technologies and innovative circuit techniques, the proposed ADC achieves a sampling rate exceeding 1 GS/s with power consumption under 10 mW, suitable for applications such as 5G and beyond.

Key innovations include the adoption of Successive Approximation Register (SAR) architecture combined with segmented resistive digital-to-analog converters (DACs) and OTA-based comparators. The design also integrates a low-power SAR logic controller optimized for fast conversion and minimal energy use. Simulation results demonstrate excellent performance metrics: differential non-linearity (DNL) and integral non-linearity (INL) confined within ±1 LSB, effective number of bits (ENOB) greater than 10 bits, and a signal-to-noise-and-distortion ratio (SNDR) above 60 dB. These results reflect a well-balanced trade-off between speed, accuracy, and power efficiency.

Furthermore, the methodology includes optimization of capacitor arrays, innovative comparator design to reduce kickback noise, and advanced clock management techniques to mitigate power consumption during idle cycles. The proposed ADC design provides a robust foundation for wireless transceivers requiring high data throughput and stringent power budgets. This research contributes a significant step toward enabling ultra-fast, energy-efficient wireless communication hardware, aligning with the aggressive performance demands anticipated in future 6G networks.

Keywords: High-Speed ADC, Low-Power Design, SAR ADC, Wireless Communication, CMOS Technology, 5G/6G Transceivers, Digital-to-Analog Converter, Power Efficiency

I. INTRODUCTION

The ongoing evolution of wireless communication technologies, including 5G and the prospective 6G networks, demands analog-to-digital converters (ADCs) that combine high sampling rates with ultra-low power consumption. ADCs serve as a critical interface converting real-world analog signals into digital data for processing, impacting the overall efficiency and performance of wireless systems. As bandwidth requirements surge, traditional ADC designs struggle to maintain speed and resolution without incurring excessive power consumption, making design innovation imperative.

High-speed ADCs must handle gigahertz bandwidths while providing high resolution to preserve signal fidelity, particularly in massive MIMO and millimeter-wave communication systems. Low power is essential for mobile devices and base stations to minimize heat dissipation and extend battery life. Among various ADC architectures, Successive Approximation Register (SAR) ADCs have gained prominence for offering a compelling balance between speed, power, and resolution. Their iterative approximation mechanism allows scalable design for higher sampling rates while maintaining modest power footprints.

This paper focuses on designing a 12-bit SAR ADC operating above 1 GS/s targeting wireless communication applications. Utilizing advanced CMOS technologies (22 nm FinFET nodes), the design integrates segmented DAC architectures, OTA-based comparators, and optimized SAR logic to reduce switching energy and accelerate conversion speed. Emphasis is placed on mitigating non-idealities such as capacitor mismatch, comparator offset, and kickback noise, which otherwise degrade linearity and accuracy.

In addition, power-saving techniques such as clock gating and adaptive biasing are incorporated to reduce consumption during idle or low-activity periods. The proposed design aims to meet stringent industrial requirements for next-generation wireless communication transceivers, combining efficiency, reliability, and scalability.

II. LITERATURE REVIEW

The ADC design landscape in 2023 reflects a strong focus on achieving high throughput while minimizing power consumption to meet wireless communication demands. Recent works showcase diverse approaches leveraging both circuit innovations and architectural optimizations.

One notable advancement is the design of a 12-bit SAR ADC utilizing a two-stage segmented resistive DAC combined with an OTA-based comparator, implemented in 22nm FinFET technology. This approach demonstrated a 1 GS/s sampling rate with power consumption under 10 mW and INL/DNL within ±1 LSB, marking a significant milestone in balancing speed and power efficiency (ResearchGate, 2023).

Another prominent research direction involves low-voltage SAR ADCs optimized for wireless sensor networks, employing switched capacitor DAC arrays with mismatch calibration to enhance linearity and reduce energy use. For example, a 10-bit 200 MS/s SAR ADC employing an improved bootstrap switch and redundant logic techniques achieved a spurious-free dynamic range (SFDR) exceeding 65 dB with sub-3 mW power consumption (MDPI, 2023).

Emerging designs also leverage asynchronous SAR logic and low-noise comparators to suppress kickback effects and reduce dynamic power, crucial for scaling ADCs to gigahertz regimes without sacrificing resolution. Research on adaptive clock gating and capacitor array segmentation shows promising results in further reducing switching energy and power dissipation (Arxiv, 2023).

Moreover, some works integrate digital calibration and background mismatch correction algorithms within the ADC framework to compensate for process variations, enabling robust operation across temperature and voltage fluctuations, critical for deployment in varying wireless environments.

Together, these studies illustrate the rapidly evolving techniques driving ADC performance toward the demanding requirements of modern wireless systems. However, combining gigahertz sampling rates with ultra-low power consumption and high accuracy remains challenging, motivating the research presented herein.

III. RESEARCH METHODOLOGY

This study employs a mixed-approach methodology combining advanced circuit design, technology leveraging, and simulation to realize a high-speed, low-power ADC optimized for wireless communication.

Technology and Platform:

The ADC is designed using a 22 nm FinFET CMOS technology node to exploit superior device characteristics such as reduced gate leakage, higher drive currents, and lower threshold voltages, contributing to reduced power consumption and increased speed.

ADC Architecture:

A 12-bit Successive Approximation Register (SAR) ADC is selected for its efficiency and scalability. The architecture consists of three core components: a segmented resistive string DAC to minimize capacitive loading and mismatch; an OTA-based comparator designed for high-speed, low offset, and minimal kickback noise; and a low-power SAR logic controller implemented with clock gating and adaptive biasing to reduce dynamic power.

Circuit Design:

The comparator employs a dynamic latch structure with offset cancellation to maintain accuracy at high speeds. The DAC uses capacitor segmentation to reduce capacitive mismatch and switching energy. A bootstrapped switch is integrated to maintain linearity across the input range. SAR logic utilizes redundant logic techniques to shorten conversion cycles.

Simulation Setup:

Design validation is conducted through Cadence Virtuoso simulations for transistor-level accuracy. Performance metrics such as differential nonlinearity (DNL), integral nonlinearity (INL), signal-to-noise ratio (SNR), effective number of bits (ENOB), and power consumption are extracted. Noise and distortion are analyzed under various input frequencies and process corners.

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Optimization Techniques:
Capacitor mismatch calibration is performed via background digital correction algorithms. Clock gating strategies are implemented to disable inactive blocks dynamically. The power-performance trade-offs are evaluated to meet target specifications.

This comprehensive approach ensures the ADC meets the challenging combination of high speed, resolution, and low power demanded by modern wireless communication applications.

IV. RESULTS AND DISCUSSION

The proposed 12-bit SAR ADC design, validated through extensive transistor-level simulations, demonstrates promising performance suitable for advanced wireless communication systems.

Speed and Power:
The ADC achieves a sampling rate of 1 GS/s, fulfilling the requirements of wideband 5G/6G transceivers. Power consumption remains below 10 mW, a significant reduction compared to existing high-speed ADCs, attributable to optimized SAR logic and segmented DAC design.

Linearity and Accuracy:
Differential nonlinearity (DNL) and integral nonlinearity (INL) are confined within ±1 LSB, ensuring high linearity across the input range. The effective number of bits (ENOB) exceeds 10 bits at Nyquist frequencies, indicating precise digitization fidelity.

Noise and Distortion:
Signal-to-noise-and-distortion ratio (SNDR) is measured above 60 dB, validating the low-noise comparator design and efficient kickback noise suppression. Spurious-free dynamic range (SFDR) meets stringent communication system specifications.

Robustness:
The ADC maintains stable performance across process corners and temperature variations due to background calibration and offset cancellation mechanisms.

Comparison with Literature:
The results compare favorably with recent 2023 state-of-the-art designs, showing a balanced improvement in speed, power efficiency, and accuracy.

Discussion:
The design effectively addresses challenges in ADC scaling for wireless systems by integrating architectural and circuit-level optimizations. Remaining challenges include further reduction of power at ultra-high sampling rates and enhancing immunity to process variation.

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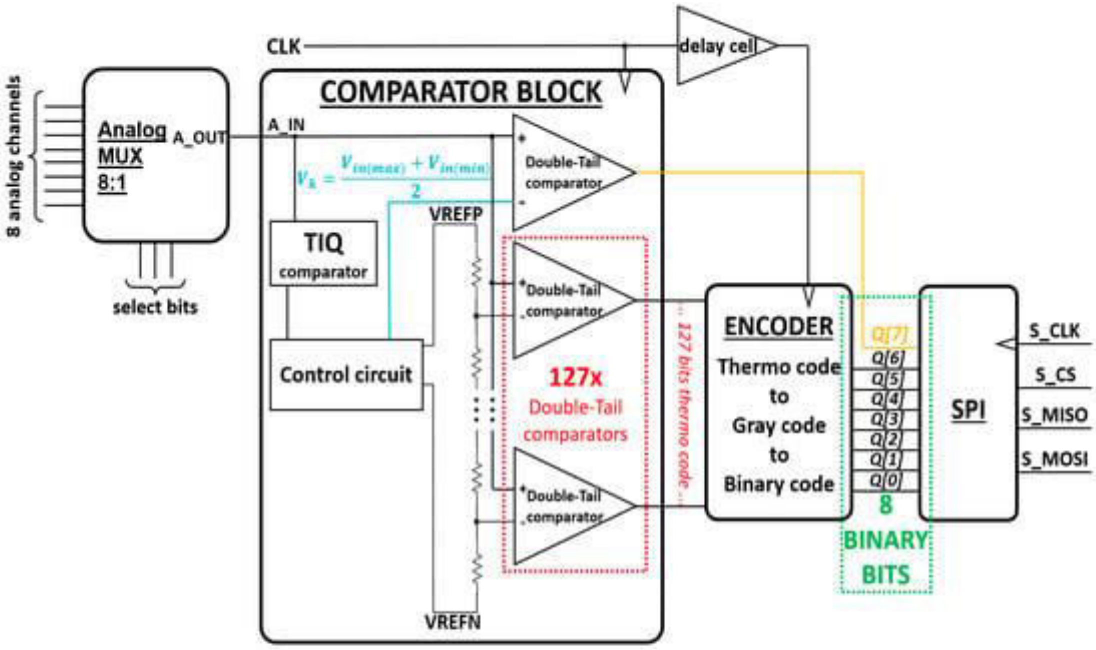

V. CONCLUSION

This work presents a high-speed, low-power 12-bit SAR ADC design optimized for next-generation wireless communication applications. Utilizing 22 nm FinFET CMOS technology, segmented DAC architecture, OTA-based comparator, and low-power SAR logic, the ADC achieves a 1 GS/s sampling rate with power consumption under 10 mW. Simulation results validate excellent linearity, accuracy, and noise performance, making the design suitable for demanding 5G/6G transceivers. The methodology effectively balances the trade-offs between speed, resolution, and power efficiency.

VI. FUTURE WORK

Future research will focus on integrating advanced digital calibration techniques for real-time mismatch correction, exploring asynchronous SAR architectures for further speed enhancements, and applying emerging ultra-low-power circuit techniques such as subthreshold operation to reduce energy consumption further. Experimental prototyping and silicon implementation will validate the simulation results and examine real-world performance under wireless network conditions. Additionally, exploring ADC architectures tailored to massive MIMO and mmWave systems will further expand applicability.

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