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Fixed-Latency, Multi-Gigabit Serial Links on FPGA using Serdes

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ABSTRACT: Most of the off-the-shelf high-speed Serializer-Deserializer (SerDes) chips do not keep the same latency through the data-path after a reset, a loss of lock or a power cycle. This implementation choice is often made because fixed-latency operations require dedicated circuitry and they are usually not needed for most telecom and data-com applications. However timing synchronization applications and triggers systems of the high energy physics experiments would benefit from fixed-latency links. In this paper, we present a link architecture based on the highspeed SerDeses embedded in Xilinx Virtex 5 and Spartan 6 Field Programmable Gate Arrays (FPGAs).We discuss the latency performance of our architecture and we show how we made it constant and predictable. We also present test results showing the fixed latency of the link and we finally offer some guidelines to exploit our solution with other SerDes devices.

KEYWORDS: Highspeed serdeses, xilink irtex 5,spartn 6,FPGAs**.**

I. INTRODUCTION

Distributed systems for data acquisition and control applications are increasingly being based on networks of multi-Gigabit serial links both on copper and optical fibers. Most of the deployed high-speed Serializers/Deserializer (SerDes) chips do not keep the same latency neither in terms of Unit Intervals (UIs, 1 UI is the duration of a serial symbol) nor in terms of parallel clock cycles after a reset, a loss of lock or a power cycle. For instance, the Texas TLK2711A [1] exhibits latency variations up to 4 UIs on the transmitter data-path and 31 UIs on the receiver side. Also, the National SCAN25100 exhibits latency variations between power-cycles, as specified in [2]. Such an implementation choice is often made because the fixed-latency operation requires dedicated circuitry and it is usually not needed for most telecom and data-com applications. However, timing synchronization and clock distribution applications would benefit from high-speed fixed-latency SerDeses. The IEEE 1588 [3] standard defines the Precision Time Protocol (PTP), which is designed for the synchronization of the clocks of a distributed system (slave clocks) to a high precision clock (the grandmaster clock). The PTP allows a system to achieve microsecond and sub-microsecond time synchronization between the clocks depending on their intrinsic precision and on the timing performance of the underlying network. A higher precision is achieved with PTP when the latency of the up-link and down-link are constant and equal. Fixed-latency links also find application in data-acquisition systems for High Energy Physics experiments, specifically in the trigger sub-systems, where it is crucial to preserve the timing information associated with the transferred signals. Trigger subsystems of experiments at the Large Hadron Collider rely on the Timing Trigger and Control [4] system developed at CERN, which distributes all the signals with predictable latency and phase. The GigaBit Transceiver (GBT) project [5], under development at CERN, is aiming at developing a unique link for data transfer, trigger and clock distribution in future Super LHC experiments. The GBT must feature deterministic latency and phase matched clock recovery. Fixed-latency serial links would also be needed for the Trigger and Data Acquisition system (TDAQ) of the SuperB [6] experiment where the links used to transport data also carry a global clock and timing information.

II. ARCHITECTURE

2.1. THE GTP TRANSCEIVER

The architecture we present in this paper is based on the GTP transceiver [13] of the Xilinx Virtex 5 FPGA family. Our concept is also compatible with the GTX transceivers available in the same family and with the GTPs embedded in

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Spartan-6 devices. Inside the FPGA, GTPs are available as configurable hard-macros (or "tiles"). Each tile includes a pair of transceivers, which share some basic components, like a Phase Locked Loop (PLL) and the reset logic.

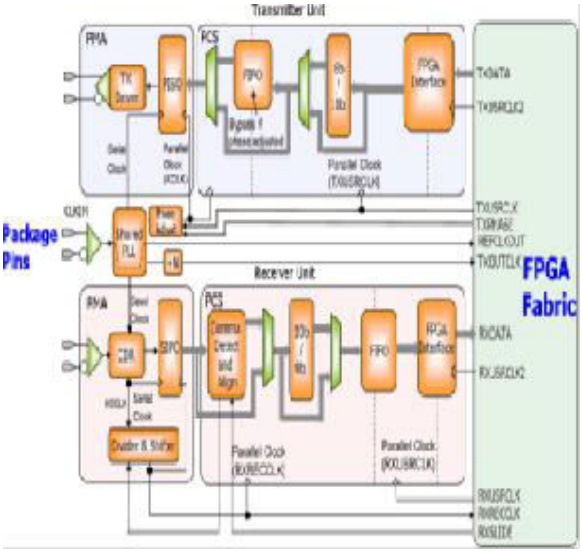

FIG 2.1 ARCHITECTURE OF TRANSMITTER AND THE RECEIVER

Fig shows the architecture of the transmitter (Tx) and the receiver (Rx) included in each transceiver. The device consists of a Physical Medium Attachment (PMA) sublayer, actually serializing and de-serializing the data, and a Physical Coding Sublayer (PCS), processing the data before serialization and after de-serialization. The shared PLL locks to a reference clock (CLKIN) and generates the high-speed serial clock for the transmitter, a seed clock for the Clock and Data Recovery (CDR) circuit and the parallel clock XCLK for the Parallel Input to Serial Output (PISO).

2.2. LATENCY VARIATIONS IN SERIAL LINKS

This paragraph briefly presents sources of latency variations in a general SerDes architecture. It is not specifically related to the GTP, yet it is useful to better understand the discussion coming in the next two sections. Latency variations may come from both the serial and parallel sections of a SerDes device.We now focus on the serial section.

Let us suppose to multiply the frequency of a clock signal ci by a factor N and let cn be the resulting signal (Fig. 2). Let us now divide the frequency of cn back by N , in order to obtain the same frequency of . There are N possible phases for cd each associated with an edge of cn(we are supposing all the clock signals to be edge-aligned). If there is data traveling from the clock domain of ci to the one of , cd the phase variation of cd leads also to a variation in latency of the data. If fixed-latency operation is required, a mechanism is needed to choose always the same phase for the divided signal and therefore also the same latency for the data.

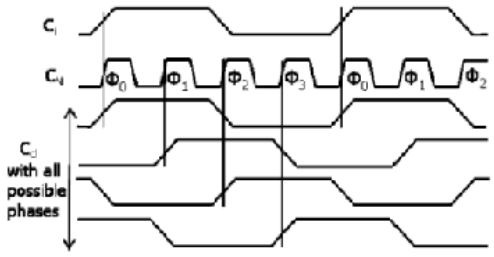

FIG 2.2 LATENCY VRIATIONS IN SERIAL LINK

2.3. GTP TRANSCEIVER

In order to support custom alignment algorithms, the GTP also allows the alignment to be driven by the logic in the FPGA fabric. A dedicated signal (RXSLIDE), when asserted, causes the parallel word to be shifted by one more bit.

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There are two modes for the bit sliding to be achieved: the first one is realized in the PCS by shifting the parallel data (PCS mode) and the second one in the PMA with a shifting of the recovered clock phase combined with the logical shifting of the data (PMA mode).

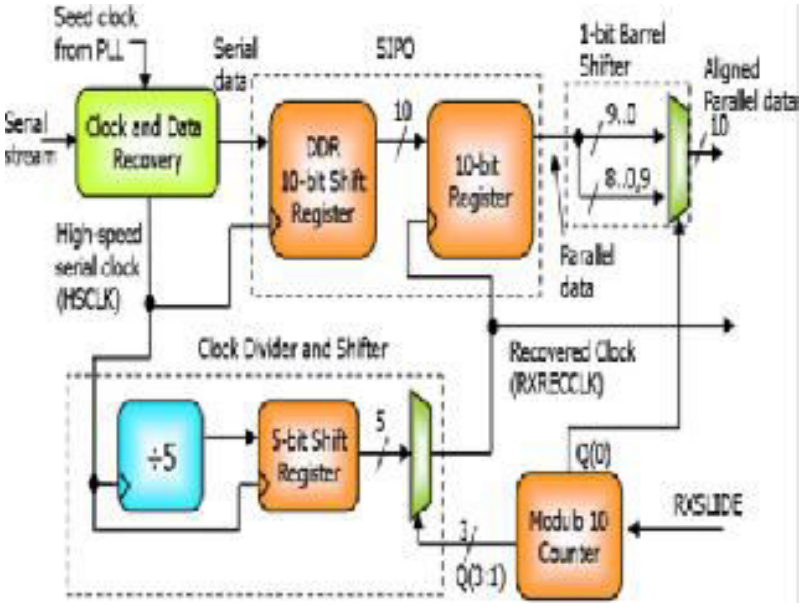

FIG 2.3 GTP TRANSCEIVER

In PCS mode, the alignment is performed logically, e.g., with a barrel shifter, and there is no way to change the phase of the recovered clock. As we stated in Section III, in order to avoid latency variations, there is the need for a mechanism capable of choosing always the same phase of the recovered clock. It follows that the PMA mode is the best candidate for fixed latency implementations. Xilinx does not disclose any information about the internal architecture of the PMA, however we propose a model of how the phase shift could be performed. We experimentally tested that the model correctly predicts the behavior of the device under the operating conditions of interest for this work. The CDR recovers a high-speed clock (HSCLK) running at half the bit-rate (UIs) and uses both edges to sample the incoming stream. A Double Data Rate (DDR) shift-register in the SIPO receives the serial data and clock from the CDR and a register re-captures the output from the shift-register on the parallel recovered clock (RXRECCLK) edge. Inside the "Clock Divider and Shifter", HSCLK is divided down by 5 and then fed in a 5-bit shift-register. The outputs of the shift-register are all separated by 1 high-speed clock cycle each (2 UIs). A modulo-10 counter, receives the RXSLIDE signal and selects which output from the shift register to use as a recovered clock. Each time a different phase from the multiplexer is selected, the recovered clock phase offset with respect to HSCLK changes. Inside the SIPO, this phase-offset determines which bit in the shift register is latched into the least significant bit (lsb) of the parallel register. Therefore, by selecting a different input in the multiplexer, the alignment of the parallel data with respect to the serial data is changed. With this model of the Clock Divider and Shifter, it is possible to shift the recovered clock phase only with steps of 2 UIs with respect to the stream. The transceiver must perform a correct logical shift for any required number of bit slips. For this reason, a 1-bit barrel-shifter receives the parallel data from the SIPO and shifts the data by 1 bit, if needed. The select signal of the multiplexer inside the barrel-shifter is driven by the LSB of the modulo-10 counter (Q(0)). On the odd RXSLIDE assertions Q(0) equals '1' and the barrel-shifter shifts the data, while on the even assertions the barrel shifter is deactivated and the data is shifted only by the shift of the recovered clock phase (Fig. 4). This way the data is always correctly shifted but for each possible recovered clock phase there are two different alignments of the parallel data, corresponding respectively to an odd and an even number of bit shifts. There is 1 UI of latency difference between the two alignments.

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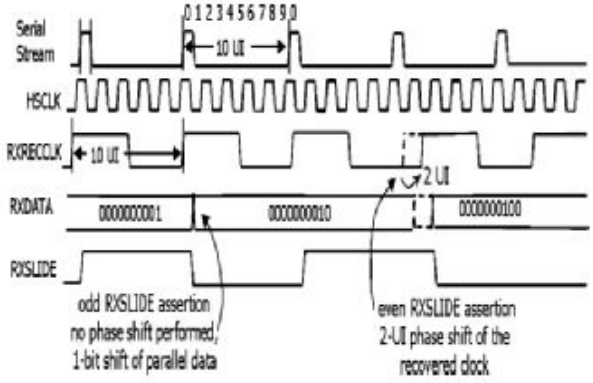

Fig. 4. Recovered clock phase adjustment by means of bit slips.

FIG 2.4 CLOCK PHASE

III. FIXED-LATENCY DATA TRANSFERS WITH THE GTP.

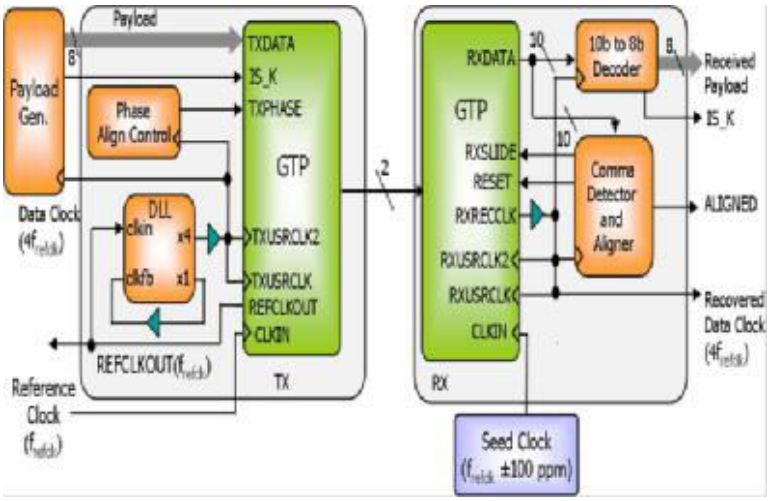

FIG 3. 1 Transmitter Unit:

3.1 Transmitter unit:

On the transmitter side, we exploit the internal 8b10b encoder and thus the GTP expects 8-bit input data words. The data generator can be programmed with a custom pattern of data and control symbols. If the IS_K input of the GTP is asserted, the incoming data is considered a control character and encoded accordingly. In this design we periodically send a K28.5 control character on the link for the receiver to find the correct byte-boundary. The CLKIN input of the PLL of the GTP receives a 62.5-MHz reference clock. In order to provide the transmit clocks, a Delay Locked Loop (DLL) external to the GTP takes the reference clock (REFCLKOUT) from the GTP and multiplies its frequency by 4, thus providing TXUSRCLK. The DLL is there to ensure the same phase offset between TXUSRCLK and REFCLKOUT at each power-up. The reason for using the REFCLKOUT output of the GTP instead of the CLKIN signal directly is that CLKIN is connected to dedicated pins of the SerDes and it is not available to the fabric. Since the parallel clock for the PISO (XCLK) is generated from the reference clock by multiplication and subsequent division, at each power-up its phase can be different. To work this issue around, we use the phase alignment circuit, which aligns the phase of XCLK to the one of TXUSRCLK. Since TXUSRCLK is generated with a deterministic phase from the reference clock, this leads to have XCLK, TXUSRCLK and the reference clock running with a deterministic fixed phase. In order

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to achieve this behavior, at each power up or after a loss of lock, a controller in the fabric activates the phase align circuit by means of the TXPHASE signal. The procedure we follow for activating the alignment circuit is the one suggested in the GTP user's guide. Under this operating condition the transmit FIFO is unnecessary and therefore we bypassed it.

3.2 Receiver Unit:

On the receiver side, the CLKIN input of the GTP is driven by a clock generator with a frequency offset smaller than 100 ppm with respect to the reference clock of the transmitter. The PLL uses this signal to generate a seed clock for the CDR to lock on the stream and correctly recover the high-speed clock. The recovered clock (RXRECCLK) drives the receive clocks (RXUSRCLK and RXUSRCLK2). In order to recover the clock always with the same phase with respect to the transmit clock, we had to deactivate the 8b10b comma detector and aligner internal to the GTP. We designed an external "Comma Detector and Aligner" in the fabric, which controls the bit sliding feature of the GTP in PMA mode. The comma detection in the fabric can be performed on the raw data (still encoded) from the transceiver. It is worth mentioning that the GTP gives access to a signal called RXBYTEISALIGNED which can be used to detect if a comma has been received on the current byte boundary, without accessing the raw data. However, this approach requires to pulse the RXSLIDE signal in a "trial-and-error" fashion until the correct alignment has been achieved.

On the contrary, with an external comma detector, we exploit the property of comma symbols in such a way to find the correct alignment at the first received comma character. Also, being the decoder external to the GTP, our approach can be customized to work with any serial encoding. In fact, we have been able to implement fixed-latency transfers between the GTP and some off-the-shelf devices, such as the Agilent G-Link chip-set [14] (supporting the conditional inversion master transition protocol) and the National Semiconductors DS92LV18 chip [15] (supporting a proprietary encoding). In order to establish a bi-unique relationship between the bit shifts performed and the corresponding recovered clock phase, it is necessary either to reject the CDR-locks leading to odd bit-shifts or to reject those leading to even bit-shifts.

Our comma detector looks for commas (e.g., the one included in the K28.5 symbol) and when it finds one it determines how many bit shifts, let it be , are required in order to align the parallel data to the correct byte boundary.

Once the comma is found, the aligner behaves according to the following algorithm:
1) If is odd the logic resets the GTP and it waits for the CDR to re-lock.
2) If is even the logic drives the RXSLIDE signal in such a way to perform an -UI shift of the clock phase and thus a -bit logical shift of the data.
The logic then asserts the ALIGNED output, flagging the correct alignment of the receiver. Data from the GTP is decoded by means of a dedicated logic and payload bits are provided as outputs on the FPGA board for test purposes. The 10b to 8b decoder also provides a flag indicating if the received word is a control character (IS_K). Its architecture is similar to the one presented in [16] and in the expired patent [17].

3.3 latencies of the transmitter and the receiver:

The latencies of the transmitter and the receiver, estimated by means of the user guide, are given in Table I. The concept proven with our design can be used to achieve fixed latency on duplex-links. In the case of independent forward and return channels, one just simply needs to use two in-stances of the architecture we proposed. In the case of a synchronous re-transmission on the return channel, some care is needed. The clock recovered by the receiver can not be directly used as a reference clock for the re-transmission. In fact, the internal PLL is shared among the transmitters and receivers in the same tile and at the receiver tile it is already locked to the seed clock. Moreover, the recovered clock might also require to be filtered in order to match the jitter specifications for the GTP reference clock. An example of such a work can be found in [18].

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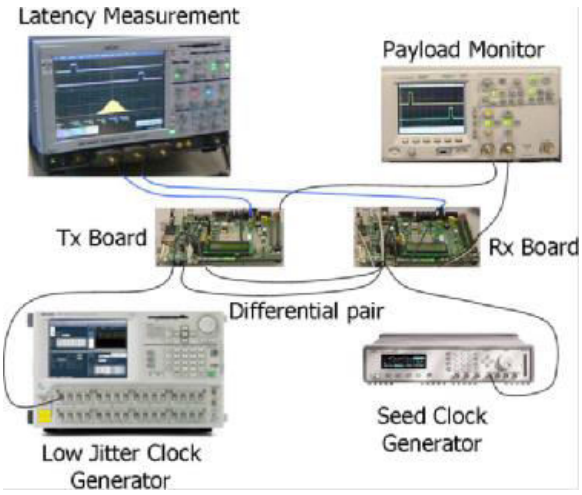
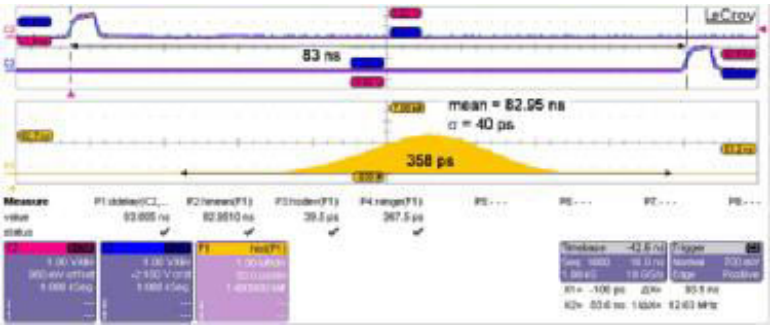
TABLE I
LATENCY OF THE INTERNAL BLOCKS OF THE TRANSMITTER AND OF THE RECEIVER

	# of RXUSRCLK cycles	Block latency (ns)
Transmitter		
FPGA Interface	1	4
8b10b Encoder	1	4
FIFO (bypassed)	1	4
Serial Section	2	8
Total Transmitter Latency	5	20
Receiver		
Serial Section	1.5	6
Comma Detector (bypassed)	3	12
FIFO	5	20
FPGA Interface	2	8
10b8b Decoder	1	4
Total Receiver Latency	12.5	50
Total Link Latency	17.5	70



3.2 Experimental setup for latency tests.

We notice that the value of the latency of our serializer and deserializer architecture is known and fixed. In some applications it might be necessary to measure in the field the latency of the link including the cables, this could be performed in a duplex link based on our architecture. Also, the proposed method is in open-loop, i.e., there is no feedback to continuously track for sub-UI latency changes and compensate for unavoidable deviations due to temperature, voltage and other parameters variations



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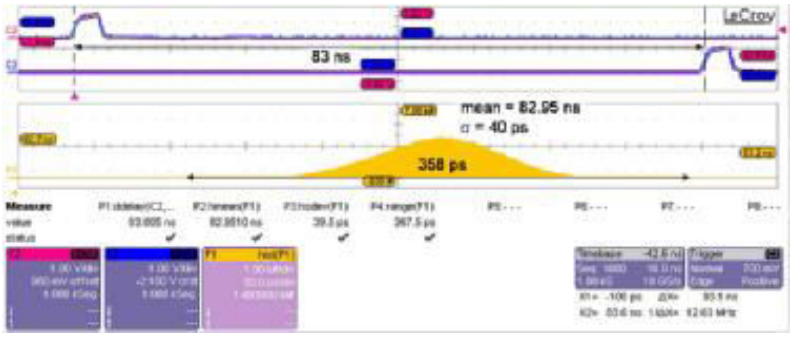

Fig. 3.2 Histogram of the latency of the link. Topmost trace: transmitted payload bit. Second trace: corresponding received bit. Down: histogram of the latency.

IV. LINK ARCHITECTURE OVERVIEW

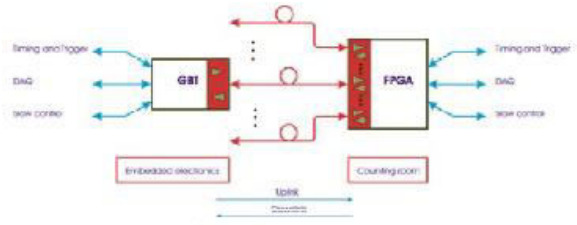

FIG 4.1 GBT BASED LINK ARCHITECTURE

4.1 Link bandwidth

As seen from its electrical interface, by the embedded electronics (and the counting room FPGA), the GBT link can be though as providing three independent interfaces with one dedicated to the DAQ, a second to the TTC, and a third to SC. All these interfaces provide a fixed bandwidth but in practice fractions of them can be assigned to different channels as will be discussed latter. To understand how the bandwidth is allocated, it is necessary to consider in detail how the data is encapsulated when transmitted between the counting room and the detectors in what is called the GBT frame. As represented schematically in Figure 2, the GBT frame is composed of 120 bits which are transmitted during a single bunch crossing interval (≅ 25 ns) resulting in a line data rate of 4.8 Gb/s. Of these, 4 bits are used for the frame Header (H) and 32 used for Forward Error Correction (FEC). This leaves a total of 84 bits free for data transmission corresponding to a user bandwidth 3.36 Gb/s. Of the 84-bits four are reserved for the SC field, the 'TTC' field is 16-bits wide and the 'D' field is 64-bits wide resulting in the following bandwidths: SC – 160 Mb/s, TTC – 640 Mb/s and DAQ – 2.56 Gb/s. The high levels of radiation (up to 1016 n/cm2 and 100 Mrd) foreseen for SLHC environments require strong error correction algorithms to be used in order to achieve error free data transmission. A significant fraction of the channel bandwidth is thus assigned to the transmission of Forward Error Correction (FEC) code. The 32-bit Error Correction (FEC) field carries an interleaved Reed-Solomon double error correction code which is discussed further.

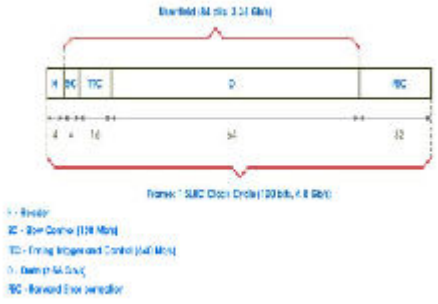

FIG 4.2 GBT FRAME

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4.2 E-Links

The full bandwidth available for data transmission might not be well matched to the requirements of a single front-end device. It is thus conceived that the GBT13 chip will connect with the Front-End ASICs through a set of 32 bi-directional serial links which are called E-Links. Typically the available bandwidth of a GBT will exceed the throughput of single front-end device being possible for a single GBT13 to serve several front-end ASICs simultaneously. The general frontend link topology using the e-links is schematized in Figure 3. Each e-link is physically implemented by three pairs of differential lines (6 wires) being them the clock (Clk+ and Clk-), Data In (Din+ and Din-) and Data Out (Dout+ and Dout-). The electrical levels follow the LVDS standard [5] and the data in both directions are simply clock synchronous to the 80 MHz clock, allowing to transmit data up to 1-2 m distance. An important feature of the GBT is that several elinks can be easily grouped together to serve a single frontend device achieving bandwidths that are multiples of 80 Mb/s.

4.3 E-link protocol

Users will connect to an e-link through a protocol that defines from the very source the packet format. It is suggested that packets of data, representing parts of physics events or multiple events, be created using the well defined Ethernet protocol. The addition of a source address and a destination address to the user data allows the construction of simple routing devices on the receiving boards in the experiment counting room and supports easily the utilization of high level software now widely in use in computers and industrial control systems. For instance, event building at the counting room level can be achieved by addressing all pieces of data of one event to a same destination, thus greatly simplifying the job of constructing the back-end of the data acquisition system.

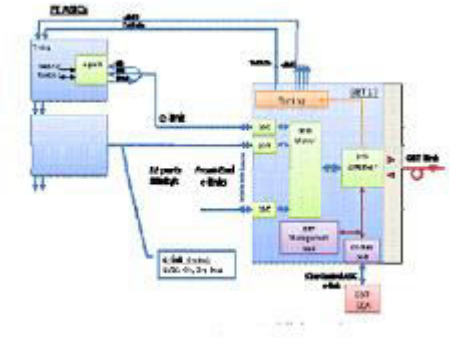

FIG 4.3 GENERAL FRONT LINK TOPOLGY

4.4 The functional principle of PTP

PTP knows two types of clocks, masters and slaves. A clock in a terminating device is known as an ordinary clock, a clock in a transmission component like an Ethernet Switch as a boundary clock. A master which is controlled ideally by a radio clock or a GPS receiver, synchronizes the respective slaves connected to it. The synchronization process is divided into two phases. First the time difference between the master and the slave is corrected, this is the offset correction. To do this, the master sends a synchronization message – SYNC message – with an estimated value of the time cyclically to the connected slaves. Parallel to this, the time at which the message leaves the sender is measured as precisely as possible, if possible by hardware support directly on the medium. The master then sends this actual exact transmission time of the corresponding sync message to the slaves in a second message - follow-up message.

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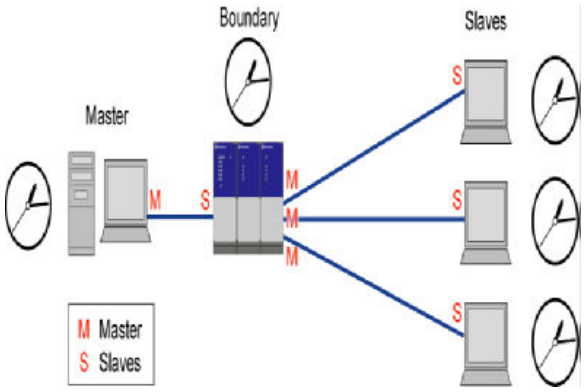

FIG 4.4 FUNCTIONAL PRINCIPAL OF PTP

These also measure the reception time of these messages as exactly as possible and can correct the correction value (offset) to the master from it. The slave clock is then corrected by this offset. If the transmission line were to have no delay, both clocks would be synchronized.

4.5 Implementation of PTP

If the Precision Time Protocol is to be used in a system, the PTP protocol stack must be implemented. This can be implemented very compactly and only makes minimum demands on the processor performance and the network bandwidth. This is very important for the implementation in simple and low-cost devices. PTP can even be implemented without any trouble in embedded systems with simple 16 or 32 bit microcontrollers. The only requirement for achieving a high precision is as exact a measurement of the PTP message transmission and reception times as possible. This must take place very close to the hardware (e.g. directly in the driver software) and with as great an accuracy as possible. In implementations as a purely software solution, therefore, the architecture and performance of the system restrict the attainable accuracy directly. When using additional hardware support for time stamping, the precision can be increased considerably and effected virtually independently of the software. A little logic is necessary for this which can be integrated, for example, as FPGA or in ASICs directly at the network input.

V. CONCLUSION

High-speed SerDes chips are typically designed for variablelatency transfers. In fact, the fixed-latency operation needs special design care and it is often not needed in most of telecom and data-com applications. However, protocols for timing synchronization and clock distribution applications, which sometime are present in HEP experiments, would benefit from fixed-latency serial links. By suitably configuring two GTP transceivers embedded in Xilinx FPGAs and adding to them a control logic in the FPGA fabric, we implemented fixed-latency operation. Our link transfers data with fixed latency and recovers the clock from the serial stream with a predictable phase, even after a reset or a power-cycle of the system. As an example of implementation, we designed a 2.5 Gbps serial link based on 8b10b encoding. Our architecture is independent of the data encoding and can be customized to support any. We highlighted the features of the GTP architecture which are crucial for the fixed latency operation and we provided some guidelines to allow the reader to use our results also with other off-the-shelf high-speed SerDeses.

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