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Low-Power RTL Design of AMBA AHB Protocol with Multi-Slave Power Management

Mr.S.Selvakumar, Haraniprabhu S, Siva M, Venkatesh J M

Assistant Professor, Department of ECE, KLN College of Engineering, Sivagangai, Tamil Nadu, India

Department of ECE, KLN College of Engineering, Sivagangai, Tamil Nadu, India

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ABSTRACT: The increasing demand for energy-efficient System-on-Chip (SoC) architectures has made power optimization a critical design constraint in modern digital systems. The Advanced Microcontroller Bus Architecture (AMBA) Advanced High-performance Bus (AHB) protocol is widely adopted for high-speed communication between processing elements and peripherals. However, continuous clock activity across AHB components leads to significant dynamic power consumption, especially during idle or low-utilization states.

This work proposes a low-power implementation of the AMBA AHB protocol using a clock gating technique to minimize unnecessary switching activity. The proposed architecture introduces selective clock control across major AHB components, including the master, slave, and arbiter modules. By dynamically enabling and disabling the clock based on transaction activity, the system effectively reduces dynamic power without compromising protocol functionality.

The design is modeled using SystemVerilog and verified through simulation using industry-standard tools. The experimental analysis demonstrates a considerable reduction in switching activity and overall dynamic power consumption compared to conventional AHB implementations. The results validate that clock gating provides an efficient and scalable solution for low-power SoC design.

KEYWORDS: Low-power RTL design, AMBA AHB protocol, multi-slave architecture, power management techniques, clock gating, dynamic power reduction, bus arbitration

I. INTRODUCTION

The rapid evolution of semiconductor technology has enabled the integration of complex functionalities into a single System-on-Chip (SoC), significantly improving performance and scalability in modern electronic systems. However, this advancement has also led to a substantial increase in power consumption, making energy efficiency a primary concern in VLSI design. In battery-operated and portable devices, excessive power dissipation not only reduces operational lifetime but also introduces thermal challenges that affect system reliability.

In contemporary SoC architectures, the on-chip communication network plays a crucial role in determining overall system performance and power characteristics. The Advanced Microcontroller Bus Architecture (AMBA), developed by ARM, has become a de facto standard for on-chip communication. Among its various protocols, the Advanced High-performance Bus (AHB) is widely adopted due to its high bandwidth, pipelined operation, and efficient burst transfer capabilities. The AHB protocol enables simultaneous address and data phases, thereby improving throughput and reducing latency in data communication between masters and slaves.

Despite these advantages, the continuous operation of the clock signal across all AHB modules leads to significant dynamic power consumption. In CMOS circuits, dynamic power is primarily caused by the charging and discharging of load capacitances during switching events. Even when modules are in an idle state, the clock signal continues to toggle, resulting in unnecessary switching activity and power wastage. This issue becomes more prominent in large-scale SoC designs where multiple modules remain inactive for considerable durations.

To address these challenges, low-power design techniques have become an essential aspect of modern VLSI systems. Among various approaches such as voltage scaling, power gating, and multi-threshold CMOS design, clock gating has emerged as one of the most effective and widely implemented methods for reducing dynamic power consumption.

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Clock gating works by selectively disabling the clock signal to inactive modules, thereby minimizing unnecessary transitions and reducing switching activity.

The integration of clock gating into bus architectures such as AHB requires careful consideration of protocol timing and synchronization constraints. Since the AHB protocol relies on strict timing relationships between control and data signals, improper clock gating can introduce glitches, data corruption, or timing violations. Therefore, a robust gating mechanism must ensure that clock control is applied only during safe idle conditions without affecting functional correctness.
In this work, the proposed AHB architecture with clock gating is modeled using SystemVerilog and functionally verified using Cadence Xcelium, an industry-standard simulation platform. The use of this tool enables accurate verification of protocol behavior, waveform analysis, and validation of clock gating logic under different operating conditions. The simulation environment ensures that the design maintains compliance with AHB specifications while achieving power optimization.

This paper presents a low-power implementation of the AMBA AHB protocol using an activity-based clock gating technique. The proposed approach focuses on identifying idle conditions within AHB transactions and dynamically controlling clock distribution to major modules, including the master, slave, and arbiter. By reducing unnecessary switching activity, the design achieves significant power savings while maintaining protocol compliance and system performance.

Furthermore, the proposed methodology emphasizes modular implementation and scalability, enabling seamless integration into existing SoC architectures. The results demonstrate that incorporating clock gating significantly enhances energy efficiency without introducing performance degradation.

The remainder of this paper is organized as follows: the next section presents the architecture of the AMBA AHB protocol, followed by the proposed methodology, implementation details, experimental results, and conclusion.

II. MATERIALS AND METHODS

The proposed research focuses on the design and implementation of a low-power AMBA AHB bus architecture using clock gating techniques. The methodology is structured into multiple stages, including architectural modeling, clock gating integration, simulation, and functional verification. The primary objective is to reduce dynamic power consumption by minimizing unnecessary clock switching while maintaining protocol compliance.

The entire system is modeled using SystemVerilog, which provides high-level abstraction and flexibility for designing complex digital systems. The simulation and verification of the proposed architecture are carried out using Cadence Xcelium, an industry-standard simulation tool that enables detailed waveform analysis and functional validation.

Unlike conventional AHB implementations where the clock signal is continuously supplied to all modules, the proposed methodology introduces activity-driven clock control. The design monitors transaction-level signals to determine module activity and dynamically enables or disables the clock signal accordingly. This approach ensures that switching activity is limited only to active modules, thereby reducing dynamic power consumption.

A. DESIGN FLOW AND DEVELOPMENT ENVIRONMENT

The development of the proposed system follows a structured RTL design methodology. Initially, the AHB architecture is defined at the register-transfer level (RTL), including master, slave, and arbiter modules. Each module is designed independently and later integrated to form the complete bus system.
The design flow includes the following stages:

RTL Modeling:
The AHB components are described using SystemVerilog, incorporating protocol-specific signals such as HADDR,

HWRITE, HTRANS, and HREADY.
Clock Gating Integration:
Clock gating logic is embedded within each module using enable-based control signals derived from transaction activity.

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Simulation Setup:
Testbenches are developed to simulate different transaction scenarios, including read, write, and idle conditions.

Functional Verification:
The design is verified using Cadence Xcelium to ensure correctness under various operating conditions.
This structured approach ensures modularity, scalability, and ease of debugging during the design process.

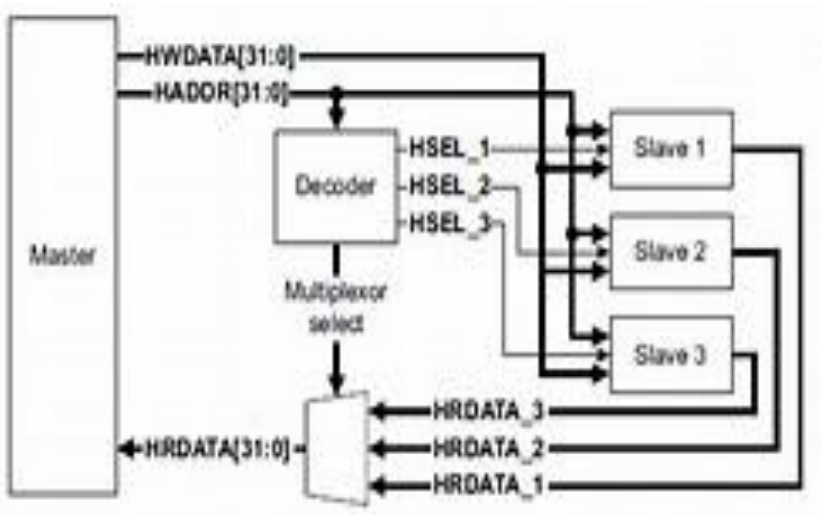
B. CLOCK GATING IMPLEMENTATION STRATEGY

The key aspect of the proposed methodology is the integration of clock gating into the AHB architecture. The gating mechanism is designed to disable the clock signal during idle conditions, thereby reducing switching activity.
The gated clock is generated using an enable-controlled logic:

$$clk_{gated} = clk \cdot enable$$

The enable signal is derived from AHB control signals, which indicate whether a module is actively participating in a transaction. For example:

- The master module is enabled only when a valid transfer is initiated
- The slave module is activated based on address decoding
- The arbiter is enabled during bus arbitration cycles



This selective clock control ensures that only active modules receive the clock signal, minimizing unnecessary transitions.

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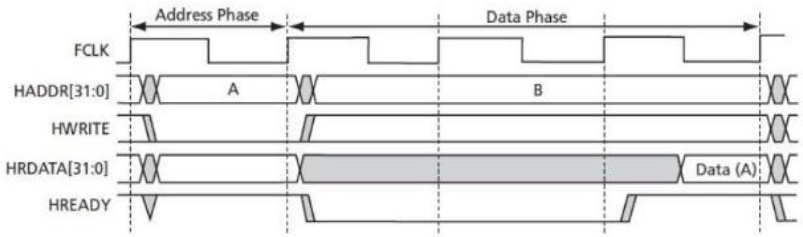

C. SYSTEM ARCHITECTURE AND MODULE DESIGN

The proposed AHB system consists of three primary modules:

AHB Master:

Generates address and control signals for data transactions. The clock is gated when no transfer request is present.

AHB Slave:

Responds to read/write operations. Clock gating is applied based on selection signals to ensure activation only during access.

AHB Arbiter:

Manages bus access among multiple masters. The arbiter remains inactive when no arbitration is required.

Each module is designed with integrated clock gating logic to ensure localized power optimization. The modular approach allows independent control of clock signals, enhancing overall efficiency.

D. SIMULATION AND TESTING METHODOLOGY

To validate the functionality of the proposed design, extensive simulations are performed using Cadence Xcelium. A comprehensive testbench is developed to evaluate system performance under various scenarios.

The test cases include:

- Single read and write transactions
- Continuous burst transfers
- Idle conditions with no bus activity
- Simultaneous requests from multiple masters

The simulation environment captures waveform outputs to analyze signal transitions, clock activity, and protocol behavior. Special attention is given to verifying that clock gating does not introduce glitches or timing violations.

E. PERFORMANCE EVALUATION APPROACH

The effectiveness of the proposed method is evaluated by comparing the clock-gated AHB design with a conventional implementation. The evaluation focuses on:

- Reduction in switching activity
- Decrease in clock transitions
- Improvement in power efficiency

The analysis is based on waveform observations and activity patterns obtained during simulation. By examining clock behavior under idle and active conditions, the impact of clock gating on dynamic power consumption is assessed.

III. EXPERIMENTAL RESULTS AND PERFORMANCE INTERPRETATION

The primary objective of the experimental evaluation is to analyze the effectiveness of the proposed clock-gated AMBA AHB architecture in reducing dynamic power consumption while maintaining functional correctness and performance. The results are obtained through detailed simulation and waveform analysis using Cadence Xcelium.

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The evaluation focuses on comparing the conventional AHB implementation with the proposed clock-gated design under identical operating conditions. Key performance indicators include switching activity, clock transitions, and overall power efficiency.

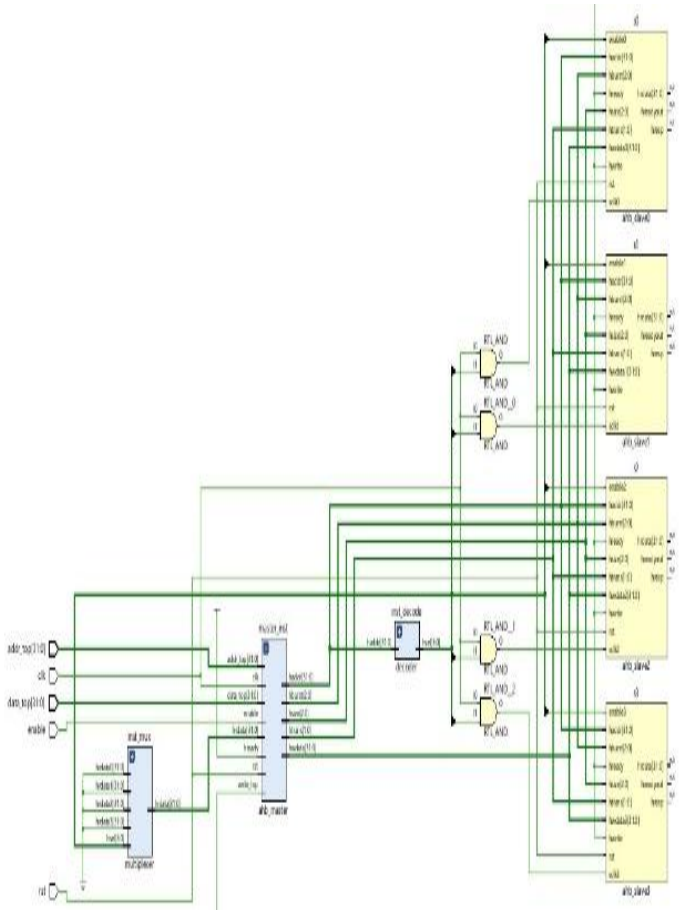
A. FUNCTIONAL VALIDATION OF AHB PROTOCOL

Before analyzing power optimization, it is essential to verify that the proposed clock-gated design maintains full compliance with the AHB protocol. Functional validation is performed by simulating multiple transaction scenarios, including read, write, burst transfers, and idle states.

The waveform analysis confirms that:

- Address and data phases are correctly aligned
- Control signals such as HREADY, HTRANS, and HWRITE operate as expected
- No data corruption or protocol violation is observed

The integration of clock gating does not interfere with the timing or sequencing of AHB transactions, ensuring reliable system operation.



B. SWITCHING ACTIVITY ANALYSIS

Switching activity is the dominant factor contributing to dynamic power consumption in digital circuits. In the conventional AHB architecture, all modules receive continuous clock signals, resulting in unnecessary transitions even during idle periods.

In contrast, the proposed clock-gated design significantly reduces switching activity by disabling the clock signal when modules are inactive. Waveform observations indicate:

- Reduced clock toggling in idle states
- Elimination of redundant transitions in inactive modules
- Controlled activation of clock signals only during valid transactions

This selective clock behavior directly contributes to lowering dynamic power consumption.

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C. POWER REDUCTION ANALYSIS

The effectiveness of clock gating is evaluated by comparing power-related parameters between the conventional and proposed designs. Although exact numerical values may vary depending on implementation, the trend clearly indicates a substantial reduction in dynamic power.

The observed improvements include:

- Noticeable decrease in clock-driven transitions
- Reduction in unnecessary capacitive charging and discharging
- Improved energy efficiency during idle and low-activity conditions

The results demonstrate that clock gating effectively minimizes dynamic power without impacting functional performance.

D. WAVEFORM-BASED INTERPRETATION

Waveform analysis plays a crucial role in understanding the behavior of the proposed system. The simulation outputs obtained from Cadence Xcelium clearly illustrate the difference between conventional and clock-gated designs.

Key observations from waveform analysis:

- In conventional design, clock signals toggle continuously across all modules
- In clock-gated design, clock activity is restricted to active modules only
- Idle modules show no switching, confirming effective gating

These observations validate that the proposed method successfully reduces unnecessary signal transitions, leading to improved power efficiency.

E. PERFORMANCE STABILITY AND TIMING ANALYSIS

A critical concern in clock gating implementation is the potential impact on system timing and performance. Improper gating can introduce glitches, clock skew, or timing violations.

However, the proposed design ensures:

- Stable clock transitions without glitches
- Proper synchronization between gated and ungated domains
- No degradation in throughput or latency

The system maintains consistent performance under all tested scenarios, indicating that the clock gating logic is correctly implemented.

F. COMPARATIVE ANALYSIS WITH CONVENTIONAL DESIGN

A comparative evaluation highlights the advantages of the proposed approach over the traditional AHB implementation.

Parameter	Conventional AHB	Clock-Gated AHB
Clock Activity	Continuous	Activity-based
Switching Activity	High	Reduced
Power Consumption	Higher	Lower
Performance	Stable	Stable

This comparison confirms that the proposed design achieves significant power savings while preserving system functionality and performance.

G. OVERALL PERFORMANCE INSIGHTS

The experimental results validate that the integration of clock gating into the AHB architecture provides a practical solution for low-power design. The reduction in switching activity directly translates to lower dynamic power consumption, making the system more energy-efficient.

Furthermore, the modular implementation ensures scalability, allowing the technique to be extended to larger and more complex SoC designs. The use of Cadence Xcelium ensures accurate verification and strengthens the reliability of the obtained results.

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IV. DISCUSSION

The results obtained from the experimental evaluation provide a comprehensive understanding of the impact of clock gating on the power efficiency of the AMBA AHB architecture. The proposed design successfully demonstrates that dynamic power consumption can be significantly reduced by minimizing unnecessary clock switching without compromising system performance or protocol compliance.

One of the key observations from this study is that switching activity plays a dominant role in overall power dissipation in bus-based architectures. In conventional AHB implementations, continuous clock distribution leads to redundant transitions across inactive modules. This unnecessary activity contributes to power wastage, particularly in scenarios where the bus remains idle for extended durations. The proposed clock-gated design effectively addresses this issue by introducing activity-driven clock control, ensuring that clock signals are propagated only when required.

From a system-level perspective, the integration of clock gating into the AHB architecture highlights the importance of localized power optimization. Instead of applying a global power reduction technique, the design selectively targets individual modules such as the master, slave, and arbiter. This modular approach enhances efficiency by reducing switching activity at the source, rather than relying solely on external power management strategies.
Another important aspect of this work is the preservation of protocol integrity. The AMBA AHB protocol is highly sensitive to timing relationships between control and data signals. Any disruption in clock synchronization can lead to data inconsistencies or functional failures. The simulation results obtained using Cadence Xcelium confirm that the proposed clock gating logic does not introduce glitches or timing violations. This indicates that the gating conditions are carefully designed to align with safe idle states within the protocol.

The waveform analysis further reinforces the effectiveness of the proposed approach. By comparing the conventional and clock-gated designs, it is evident that the latter exhibits significantly reduced clock transitions during inactive periods. This reduction directly correlates with lower dynamic power consumption, validating the theoretical relationship between switching activity and power dissipation in CMOS circuits.

In addition to power savings, the proposed design maintains stable performance characteristics. Metrics such as throughput and latency remain unaffected, demonstrating that power optimization has been achieved without introducing performance trade-offs. This balance between efficiency and performance is critical for modern SoC applications, where both parameters are equally important.

From a scalability standpoint, the proposed methodology offers significant advantages. The clock gating technique can be extended to more complex bus architectures or integrated into larger SoC designs with multiple subsystems. The modular nature of the implementation allows designers to incorporate additional gating logic without major structural modifications.

However, certain challenges must be considered when implementing clock gating in practical systems. The design of enable signals requires careful analysis to avoid incorrect gating conditions. Additionally, excessive gating logic may introduce design complexity and increase area overhead. Therefore, an optimal balance must be maintained between power savings and hardware cost.

Overall, the study demonstrates that clock gating is a highly effective and practical solution for reducing dynamic power consumption in AHB-based systems. By combining theoretical principles with simulation-based validation, the proposed approach provides a reliable framework for low-power VLSI design. The use of Cadence Xcelium further strengthens the credibility of the results by ensuring accurate functional verification and waveform analysis.

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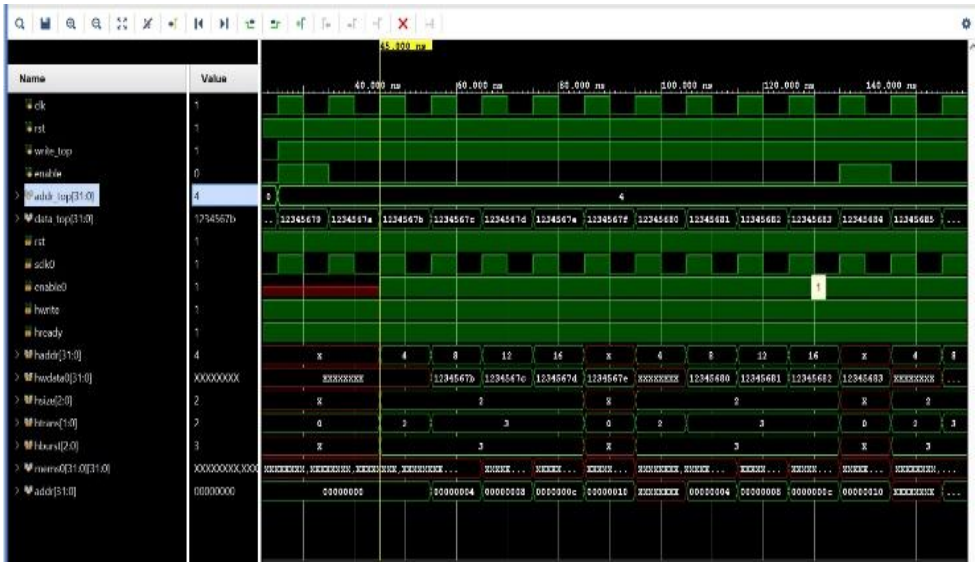

V. CONCLUSION

This paper presents a comprehensive low-power implementation of the AMBA AHB protocol using an activity-driven clock gating technique aimed at reducing dynamic power consumption in modern System-on-Chip (SoC) architectures. With the increasing demand for energy-efficient digital systems, particularly in portable and battery-operated devices, minimizing power dissipation at the architectural level has become a critical design objective. The proposed approach addresses this challenge by targeting one of the primary contributors to power consumption—unnecessary clock switching.

The study begins by identifying the limitations of conventional AHB implementations, where continuous clock distribution results in redundant switching activity even during idle conditions. This inefficiency becomes more pronounced in complex SoC environments, where multiple modules remain inactive for extended periods. By integrating clock gating into the AHB architecture, the proposed design effectively eliminates such redundant transitions by enabling clock signals only when required.

The implementation is carried out using SystemVerilog, and the design is functionally verified using Cadence Xcelium to ensure compliance with AHB protocol specifications. Extensive simulation results confirm that the proposed clock-gated design maintains correct functionality across various operational scenarios, including read, write, burst, and idle states. The waveform analysis demonstrates stable clock behavior without glitches, indicating that the gating logic is carefully synchronized with the system's timing requirements.

A detailed performance evaluation highlights a significant reduction in switching activity compared to the conventional design. Since dynamic power in CMOS circuits is directly proportional to switching frequency, this reduction translates into improved energy efficiency. The results clearly validate that clock gating is an effective technique for minimizing dynamic power consumption without introducing any degradation in system performance. Key parameters such as throughput and latency remain unaffected, ensuring that the design achieves an optimal balance between power efficiency and operational speed.

One of the notable strengths of the proposed methodology is its modular and scalable nature. The clock gating mechanism is applied independently to major AHB components, including the master, slave, and arbiter modules. This localized approach allows for fine-grained control of clock signals and can be easily extended to larger and more complex SoC architectures. The design framework can also be adapted to other AMBA protocols or integrated with additional low-power techniques for further optimization.

Furthermore, this work emphasizes the practical feasibility of implementing clock gating in real-world VLSI systems. The use of Cadence Xcelium ensures accurate validation of both functional and timing aspects, thereby strengthening the reliability of the proposed design. The results obtained from simulation closely align with theoretical expectations, reinforcing the effectiveness of reducing switching activity as a primary strategy for power optimization.

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Despite its advantages, the study also acknowledges certain design considerations. The generation of accurate enable signals is critical to ensure proper clock gating without affecting system stability. Additionally, the inclusion of gating logic introduces minor design overhead, which must be carefully managed during implementation. However, these challenges are outweighed by the substantial power savings achieved through the proposed approach.

In conclusion, the integration of clock gating into the AMBA AHB architecture provides a robust and efficient solution for low-power SoC design. The proposed method successfully reduces dynamic power consumption by minimizing unnecessary clock activity while maintaining full protocol compliance and performance integrity. This work contributes to the growing field of energy-efficient VLSI design and offers a scalable framework that can be extended to future high-performance, low-power applications.

VI. FUTURE SCOPE

The proposed clock-gated AMBA AHB architecture provides an effective foundation for low-power SoC design; however, several enhancements can be explored to further improve power efficiency and system performance. Future work can focus on integrating advanced power optimization techniques alongside clock gating to achieve multi-level power reduction. One potential extension is the incorporation of **power gating**, where entire modules can be completely shut down during prolonged idle periods. Unlike clock gating, which reduces dynamic power, power gating can significantly reduce leakage power, making it highly suitable for deep submicron technologies.

Another promising direction is the implementation of **adaptive or intelligent clock gating mechanisms**, where enable signals are dynamically generated based on real-time workload conditions. Machine learning-based prediction models can be explored to identify usage patterns and optimize clock control more efficiently. The proposed design can also be extended to more advanced AMBA protocols such as **AXI (Advanced eXtensible Interface)**, which supports higher bandwidth and out-of-order transactions. Applying clock gating in such complex architectures would further validate the scalability and robustness of the approach. In addition, future work may include **hardware synthesis and FPGA prototyping** to evaluate real-time performance, area overhead, and power consumption under practical conditions. This would provide more accurate insights beyond simulation-based analysis performed using Cadence Xcelium. Further optimization can be achieved by exploring **fine-grained clock gating techniques**, where gating is applied at sub-module or register levels. This can lead to even greater reduction in switching activity, although it requires careful design to avoid timing complexity. Finally, the integration of the proposed low-power AHB architecture into complete SoC systems, including processors and memory subsystems, can be investigated. This would enable the evaluation of system-level power savings and demonstrate the practical applicability of the design in real-world embedded and high-performance computing applications.

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