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A Novel Vedic Multiplication for High Speed Systems using Quantum-dot Cellular Automata

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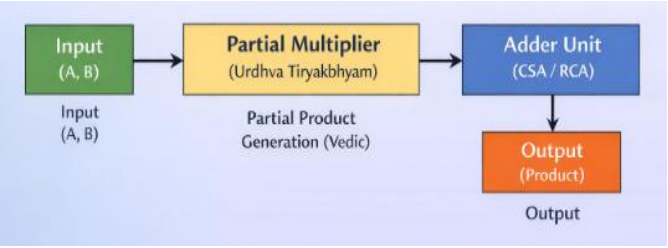
ABSTRACT: As the scaling limitations of conventional CMOS technology increasingly affect power efficiency and performance, alternative nano-scale computing paradigms have emerged as promising solutions. Quantum-dot Cellular Automata (QCA) is a post-CMOS technology that represents binary information through electron polarization rather than current flow, enabling ultra-low power dissipation and high-speed operation. In parallel, Vedic multiplication based on the Urdhva Tiryagbhyam sutra offers an efficient arithmetic technique by enabling parallel generation of partial products.

The Vedic multiplication algorithm is systematically translated into logical expressions and implemented using QCA majority gates and inverters with appropriate clocking schemes. The proposed architecture exploits the inherent parallelism of the Vedic sutra to reduce computational delay and circuit complexity. The design is modeled and simulated using QCA Designer to verify functional correctness.

Simulation results demonstrate that the proposed QCA-based Vedic multiplier achieves improved speed and reduced structural complexity compared to conventional CMOS-based multiplier architectures. Due to its low-power operation and parallel processing capability, the proposed design is well suited for high-speed arithmetic units in future nano-scale and energy-efficient computing systems.

KEYWORDS: QCA, Vedic Multiplier, Urdhva Tiryagbhyam, Majority Gate, Low Power, Nano-scale Computing



I. INTRODUCTION

With the continuous advancement of semiconductor technology, conventional CMOS-based digital circuits are approaching their fundamental scaling limits. As device dimensions shrink into the nanometer regime, several challenges such as increased power dissipation, leakage currents, short-channel effects, and interconnect delays significantly affect system performance and reliability. These limitations have motivated researchers to explore alternative nano-scale computing paradigms that can overcome the drawbacks of traditional CMOS technology.

Quantum-dot Cellular Automata (QCA) has emerged as a promising post-CMOS technology that offers a novel approach to digital computation. Unlike conventional transistor-based systems, QCA represents binary information using the polarization of electrons within quantum cells rather than current flow. This unique mechanism enables ultra-low power dissipation, high device density, and fast switching speeds. In QCA, computation is performed through the interaction of neighboring cells, eliminating the need for complex interconnections and reducing energy consumption significantly. The fundamental building block of QCA circuits is the majority gate, which provides a flexible and efficient way to implement various logic functions.

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In parallel, efficient arithmetic operations play a crucial role in digital systems such as processors, signal processing units, and embedded systems. Multiplication is one of the most important and frequently used arithmetic operations, and its performance directly impacts overall system efficiency. Vedic mathematics, an ancient system of mathematical techniques, provides efficient algorithms for arithmetic computations. Among these, the Urdhva Tiryagbhyam (vertical and crosswise) method is widely used for multiplication due to its ability to generate partial products in parallel, thereby reducing computational delay and improving speed.

The integration of QCA technology with Vedic multiplication algorithms provides an effective solution for designing high-speed and low-power arithmetic circuits. By exploiting the inherent parallelism of the Urdhva Tiryagbhyam method and the efficient logic implementation capability of QCA majority gates, it is possible to achieve optimized circuit performance with reduced complexity.

In this work, a 2×2 Vedic multiplier is designed and implemented using QCA technology. The proposed design utilizes majority gates and inverters to realize logical operations, along with a proper clocking scheme to ensure controlled signal propagation. The multiplication process is carried out by generating partial products and combining them using XOR and majority logic structures. The circuit is modeled and simulated using QCA Designer to verify its functional correctness.

The proposed system demonstrates stable polarization behavior and correct output for all input combinations. Additionally, the design achieves ultra-low power consumption in the pico-watt range, highlighting the efficiency of QCA technology. The main contribution of this work is the development of a compact, low-power, and high-speed Vedic multiplier using QCA, which is suitable for future nano-scale and energy-efficient computing applications.

II. RELATED WORK

Recent advancements in nano-scale computing technologies have highlighted the limitations of conventional CMOS-based digital systems, particularly in terms of power consumption, device scaling, and interconnect complexity. As a result, alternative computing paradigms such as Quantum-dot Cellular Automata (QCA) have gained significant attention for implementing digital logic circuits with ultra-low power dissipation and high device density. QCA technology replaces current-based switching with electron polarization, enabling efficient computation at the nano-scale level.

In the field of arithmetic circuit design, multipliers play a crucial role in digital signal processing, image processing, and embedded systems. Conventional multiplier architectures such as array multipliers and Booth multipliers have been widely implemented using CMOS technology. However, these designs suffer from high power consumption, increased delay, and larger area when scaled down to nano dimensions. To address these challenges, researchers have explored QCA-based implementations of arithmetic circuits, which offer reduced power consumption and compact design.

Several works have focused on designing QCA-based adders and multipliers using majority gates and optimized clocking schemes. Majority gate-based logic design simplifies circuit implementation and reduces the number of required components. In particular, QCA-based half adders and full adders have been extensively studied as fundamental building blocks for multiplier design. However, many existing QCA multiplier designs still face challenges such as increased cell count, complex wire crossings, and inefficient clocking arrangements, which can affect overall performance and stability.

In parallel, Vedic mathematics has been widely explored for designing efficient arithmetic circuits. The Urdhva Tiryagbhyam (vertical and crosswise) algorithm is especially popular due to its ability to generate partial products in parallel, thereby reducing computation time. Several CMOS-based Vedic multipliers have demonstrated improved speed compared to conventional multipliers. However, when implemented in CMOS, they still suffer from power and scaling limitations.

Recent research efforts have combined QCA technology with Vedic multiplication techniques to exploit the advantages of both approaches. These designs aim to achieve high-speed operation through parallel computation while maintaining low power consumption using QCA logic. However, many of the existing implementations are either complex in structure or not fully optimized in terms of cell arrangement and clocking.

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Therefore, there is a need for a simplified and efficient QCA-based Vedic multiplier design that minimizes structural complexity while maintaining correct functionality and low power consumption. This work focuses on the design and implementation of a 2×2 Vedic multiplier using QCA, with optimized majority gate logic and proper clocking, ensuring stable operation and improved performance.

III. EXISTING METHOLOGY

Most existing multiplier designs generate partial products using AND gates and combine them using adders such as half adders and full adders. While these architectures are widely used due to their reliability and ease of implementation, they suffer from several limitations when scaled to nano-scale dimensions. As transistor sizes decrease, issues such as leakage current, increased power dissipation, interconnect delay, and heat generation become significant challenges. These factors negatively impact the performance, efficiency, and scalability of CMOS-based multiplier circuits.

In addition, conventional multiplier architectures typically follow sequential or partially parallel approaches, which introduce additional propagation delay and limit computational speed. Although advanced techniques such as pipelining and parallel processing have been introduced to improve performance, they often result in increased circuit complexity and area.

Furthermore, traditional CMOS-based designs lack energy efficiency when compared to emerging nano-scale technologies. The continuous charging and discharging of capacitive loads during switching leads to higher dynamic power consumption. This makes conventional multipliers less suitable for applications requiring ultra-low power operation.

Although some research efforts have explored alternative implementations using emerging technologies, many existing designs are still complex, require a large number of components, and are not optimized for minimal power consumption or compact layout. Additionally, issues such as signal delay, wiring complexity, and scalability remain significant concerns.

Therefore, while existing multiplier methodologies are well-established and widely used, they are not ideal for future nano-scale and energy-efficient computing systems. These limitations highlight the need for alternative approaches such as QCA-based designs, which can overcome the drawbacks of conventional CMOS implementations.

IV. SYSTEM ARCHITECTURE

OVERVIEW

The architecture follows the Urdhva Tiryagbhyam multiplication method, where partial products are generated in parallel and combined using majority gate logic. The design consists of QCA cells, majority gates, inverters, and properly arranged clock zones to ensure controlled and synchronized signal propagation. The computation is performed in a structured manner, where input signals are applied, processed through logic blocks, and propagated across clock phases to produce the final output. The system operates using a clock-driven mechanism, where each stage of computation is controlled by a four-phase clocking scheme. This ensures stable data flow, avoids signal interference, and maintains proper timing between different logic stages. The output is obtained in terms of cell polarization, which directly represents the binary multiplication result. The proposed architecture ensures efficient utilization of QCA resources, reduced circuit complexity, and reliable operation. It is modeled and simulated using QCA Designer to verify functional correctness and performance under different input conditions.

Hardware Platform

The primary hardware component used is an FPGA development board, which acts as the processing unit for implementing the Vedic multiplier logic. The multiplier is designed using a Hardware Description Language (HDL) such as Verilog or VHDL and synthesized onto the FPGA. The FPGA provides a reconfigurable platform that enables real-time testing and validation of the multiplier operation. Input signals corresponding to A1, A0, B1, and B0 are applied through switches available on the FPGA board, while the output signals (P3, P2, P1, P0) are observed using onboard LEDs or display modules.

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The FPGA implementation replicates the logical behavior of the Vedic multiplication algorithm, where partial products are generated and combined using combinational logic. This provides a practical validation of the multiplier design in a hardware environment, ensuring correctness beyond simulation.

In addition to the FPGA implementation, the design is also modeled using QCA Designer to represent the nano-scale realization of the circuit. The QCA layout consists of standard 4-dot cells, majority gates, inverters, and clocking zones, which together perform the multiplication operation based on electron polarization. The simulation tool is used to analyze polarization behavior, signal propagation, and functional correctness.

Software Platform

The proposed system is designed and simulated using QCA Designer-E, which provides a graphical environment for modeling QCA circuits. The 2×2 Vedic multiplier is implemented using QCA cells, majority gates, inverters, and proper clock zones for controlled signal propagation.

Input polarizations (A1, A0, B1, B0) are assigned, and the output is observed based on cell polarization values. The tool simulates electron interactions and displays waveform results to verify correct functionality.

The simulation confirms stable outputs (+1 and −1) for all input combinations and enables analysis of signal propagation and power characteristics, making QCA Designer-E suitable for validating the proposed design.

V. PROPOSED METHODOLOGY

The proposed system presents a QCA-based implementation of a 2×2 Vedic multiplier designed for nano-scale, low-power arithmetic applications. The primary objective of the system is to perform efficient binary multiplication using the Urdhva Tiryagbhyam algorithm while minimizing power consumption and circuit complexity. The design operates based on electron polarization rather than current flow, enabling ultra-low energy dissipation and high-speed computation.

The system begins with the application of binary input values A1, A0, B1, and B0, which are assigned as polarization states (+1 for logic ‘1’ and −1 for logic ‘0’) in the input QCA cells. These inputs are propagated through QCA wires, where neighboring cell interactions transfer polarization across the circuit. The multiplication process follows the Vedic method, where partial products are generated in parallel. Specifically, four AND operations are performed to obtain A0B0, A1B0, A0B1, and A1B1. These operations are implemented using QCA majority gates by fixing one input to logic ‘0’.

To compute the intermediate results, cross products A1B0 and A0B1 are combined using XOR logic, which is realized through a combination of majority gates and inverters. This produces the second output bit (P1) and an associated carry. The carry generated from this stage is then combined with the partial product A1B1 using another XOR operation to produce P2, while a final carry operation generates the most significant bit (P3). The least significant bit (P0) is directly obtained from A0B0.

The entire computation is controlled using a four-phase clocking scheme, which ensures synchronized signal propagation across different regions of the circuit. Each stage of the multiplier is assigned to a specific clock zone, allowing sequential and stable data flow. This clock-controlled mechanism prevents signal interference and ensures correct timing behavior throughout the operation.

The proposed design is modeled and simulated using QCA Designer-E, where the layout is constructed using standard 4-dot QCA cells, majority gates, and inverters. The simulation process involves assigning input polarization values and observing output polarization to verify correctness. Waveform analysis is performed to ensure that the outputs follow expected multiplication results for all input combinations.

Overall, the proposed methodology demonstrates an efficient approach to implementing a Vedic multiplier using QCA technology. By combining parallel computation with majority logic and controlled clocking, the system achieves reduced complexity, high-speed operation, and ultra-low power consumption, making it suitable for future nano-scale computing applications.

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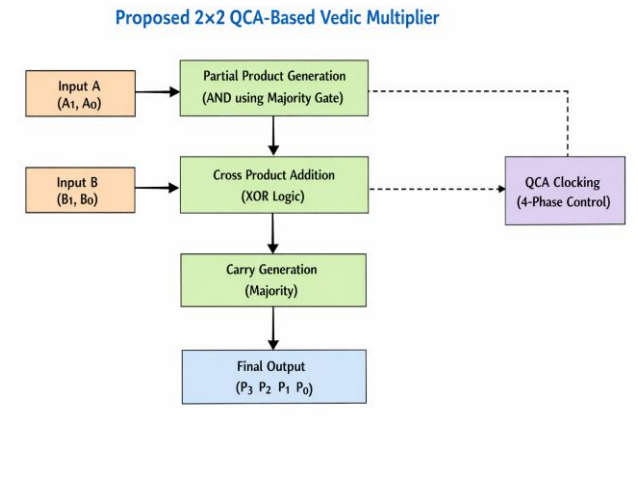

Fig.1. Proposed System Block Diagram

VI. METHODOLOGY EQUATIONS

The proposed system implements a 2×2 Vedic multiplier using Quantum-dot Cellular Automata (QCA), where computation is performed based on cell polarization and majority logic. The operation of the multiplier is governed by logical relationships derived from the Urdhva Tiryagbhyam algorithm, which enables parallel generation of partial products.

The fundamental operation in QCA is the majority gate, which is mathematically expressed as:

$$M(A,B,C) = AB + BC + CA$$

By fixing one of the inputs to a constant polarization, basic logic functions can be derived. The AND and OR operations are implemented as:

$$AND(A,B) = M(A,B,0)$$
$$OR(A,B) = M(A,B,1)$$

The NOT operation is achieved using an inverter structure:

$$A' = NOT(A)$$

Using these basic operations, the Vedic multiplication process is formulated. For two 2-bit inputs:

$$A = A_1A_0, B = B_1B_0$$

The partial products are generated as:

$$P_0 = A_0 \cdot B_0$$
$$X_1 = A_1 \cdot B_0$$
$$X_2 = A_0 \cdot B_1$$
$$X_3 = A_1 \cdot B_1$$

The intermediate sum and carry are computed using XOR and majority logic:

$$P_1 = X_1 \oplus X_2$$
$$C_1 = X_1 \cdot X_2$$

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The next stage combines the carry with the final partial product:

$$P_2 = C_1 \oplus X_3$$
$$P_3 = C_1 \cdot X_3$$

The XOR operation in QCA is implemented using majority gates and inverters as:

$$A \oplus B = M(M(A', B, 1), M(A, B', 1), 0)$$

The entire computation is controlled using a four-phase clocking mechanism, which ensures sequential signal propagation across the circuit. Each stage of the multiplier operates in a different clock zone, maintaining synchronization and stable polarization transfer.

Thus, the proposed methodology combines majority gate logic, inverter-based complementation, and structured clocking to realize efficient multiplication. The use of polarization-based computation enables ultra-low power operation while maintaining correct logical functionality.

VII. RESULTS AND DISCUSSION

The proposed QCA-based 2×2 Vedic multiplier was designed and simulated using QCA Designer-E to evaluate its functional performance and correctness. The circuit was tested for all possible input combinations of A1A0 and B1B0 (00 to 11), and the corresponding output bits (P3, P2, P1, P0) were observed through waveform analysis.

The simulation results show that the multiplier produces correct outputs for all input conditions. The polarization values of the output cells remain stable, where +1 represents logic '1' and −1 represents logic '0'. The outputs follow the expected binary multiplication results, confirming the correctness of the implemented Vedic multiplication algorithm. The performance of the system is summarized in Table 1.

Table 1: Output Performance of 2×2 Vedic Multiplier

Inputs (A1A0 × B1B0)	Output (P3 P2 P1 P0)
00 × 00	0000
01 × 01	0001
10 × 10	0100
11 × 11	1001

The simulation demonstrates proper signal propagation across different clock zones, ensuring synchronized operation of the circuit. The outputs exhibit clear transitions without instability, indicating correct clocking and layout design. Additionally, the energy dissipation observed is in the pico-watt range, confirming the ultra-low power nature of QCA technology.

The design also shows reduced complexity due to the use of majority gate logic and parallel computation inherent in the Vedic multiplication method.

Discussion

The results confirm that the proposed system successfully implements a 2×2 Vedic multiplier using QCA technology with correct logical functionality. Compared to conventional CMOS-based multipliers, the design offers significant advantages in terms of power efficiency, compactness, and scalability. The use of the Urdhva Tiryagbhyam algorithm enables parallel generation of partial products, reducing computation delay.

Majority gate-based implementation further simplifies the circuit structure and minimizes the number of required components. Although the design performs correctly in simulation, minor variations in polarization levels may occur due to factors such as cell interaction strength, clocking delays, and layout arrangement. Additionally, complex wire crossings and improper clock zone assignments can affect signal integrity if not carefully designed.

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However, for nano-scale arithmetic applications, the proposed design provides reliable performance with low power consumption and efficient operation. The results demonstrate that QCA-based Vedic multipliers are a promising alternative for future high-speed and energy-efficient computing systems.

IX. CONCLUSION

In this work, a QCA-based 2×2 Vedic multiplier has been successfully designed and implemented for nano-scale arithmetic applications. The primary objective of the system was to achieve efficient multiplication with reduced power consumption and improved computational speed compared to conventional CMOS-based designs. The proposed system effectively addresses the limitations of traditional technologies by utilizing electron polarization and majority gate logic for computation.

The design integrates the Urdhva Tiryagbhyam Vedic multiplication algorithm with QCA technology to enable parallel generation of partial products. The use of majority gates and inverters simplifies the logic implementation, while the structured clocking scheme ensures proper signal propagation and synchronization across the circuit. The entire system is modeled and simulated using QCA Designer-E, enabling accurate analysis of polarization behavior and functional performance.

Simulation results demonstrate that the proposed multiplier produces correct outputs for all input combinations, with stable polarization levels representing binary logic values. The design shows efficient operation with ultra-low power dissipation in the pico-watt range, highlighting the energy-efficient nature of QCA technology. Additionally, the circuit achieves reduced structural complexity and compact layout compared to conventional multiplier architectures.

Compared to CMOS-based implementations, the proposed QCA design offers significant advantages such as lower power consumption, higher device density, and faster operation due to parallel processing. Although the design is validated through simulation, practical implementation challenges such as fabrication complexity, temperature sensitivity, and precise clocking control need to be addressed for real-world applications.

Overall, the proposed QCA-based Vedic multiplier presents a compact, low-power, and high-speed solution for future nano-scale computing systems. It also demonstrates the potential of combining Vedic arithmetic techniques with emerging QCA technology, providing a strong foundation for further research in advanced digital circuit design and energy-efficient computation.

Furthermore, the proposed design demonstrates the effectiveness of QCA technology in implementing arithmetic circuits with minimal energy dissipation and high computational efficiency. The use of structured clock zones ensures proper data synchronization and reliable signal propagation across different stages of the circuit, which is crucial for stable operation in QCA systems.

The design also highlights the advantage of parallel computation offered by the Vedic multiplication technique, which reduces overall latency compared to conventional sequential multiplier architectures. This makes the proposed system suitable for high-speed arithmetic units in advanced computing applications such as digital signal processing, image processing, and embedded nano-scale systems.

In addition, the compact layout and reduced cell count contribute to area efficiency, making the design scalable for higher-order multipliers. The methodology adopted in this work can be extended to implement larger multipliers (such as 4×4 or 8×8) and other complex arithmetic circuits using QCA technology.

Overall, this work not only validates the functionality of a QCA-based Vedic multiplier but also establishes its potential as a key building block for next-generation low-power and high-speed computing architectures.

X. FUTURE SCOPE

The proposed QCA-based Vedic multiplier can be further enhanced to improve performance, scalability, and applicability in advanced nano-scale computing systems. Future developments may include:

- ¬ Extension of the design to higher-order multipliers such as 4×4, 8×8, and beyond for complex arithmetic operations
- ¬ Optimization of QCA layout to reduce cell count, area, and wire crossings for improved efficiency

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- ¬ Implementation of multilayer QCA structures to overcome planar design limitations and enhance circuit density
- ¬ Integration of the multiplier into larger systems such as Arithmetic Logic Units (ALUs) and digital processors
- ¬ Exploration of advanced clocking techniques to reduce delay and improve synchronization
- ¬ Incorporation of fault-tolerant and error-resilient design methods to improve reliability in nano-scale environments
- ¬ Analysis and optimization of power dissipation using advanced QCA simulation tools
- ¬ Investigation of practical fabrication techniques for real-world implementation of QCA circuits

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