International Journal of Engineering & Extended Technologies Research (IJEETR)

|ISSN: 2322-0163| www.ijeetr.com | A Bimonthly, Peer Reviewed, Scholarly Indexed Journal |

| Volume 8, Issue 2, March - April 2026 |

DOI:10.15662/IJEETR.2026.0802080

FPGA-Based Real-Time Image Edge Detection using Pipelined Sobel and Canny Operations

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Publication History: Received: 25.02.2026; Revised: 20.03.2026; Accepted: 25.03. 2026; Published: 28.03.2026.

ABSTRACT: Image edge detection is a fundamental requirement in applications like surveillance, robotics, medical imaging, and intelligent transportation. Sobel is fast, simple, hardware-friendly operator which has some smoothing effect due to small averaging window for more noise-resistant. Canny operator provides good accuracy for edge detection to produce sharper and cleaner edges by applying gaussian smoothing. An efficient FPGA- based architecture for real-time image edge detection using combined Sobel and Canny operators with improvement using adaptive thresholding and morphological clean-up with a fully pipelined, streaming hardware approach, enabling continuous pixel-level processing with minimal latency is proposed. The Sobel operator is used to extract gradient components (Gx, Gy) with optimized fixed-point arithmetic and Canny operator to improve accuracy and latency. The designs are modeled in Verilog HDL and Zynq 7000 Series FPGA is used for implementation. The simulation results confirm that the combination of Sobel's low-cost gradient extraction with Canny's superior edge refinement provides 5.7% to 62.5%.

KEYWORDS: Real-Time Image Processing, Edge Detection, Sobel Operator, Canny Edge Detection, FPGA Implementation.

I. INTRODUCTION

Finding notable intensity changes that correspond to object boundaries, surface discontinuities, and structural elements inside an image is the goal of edge detection. These edges are used for vision tasks such as object detection, feature extraction, image segmentation, tracking and scene interpretation. The requirements include high detection accuracy, immune to noise for applications like surveillance systems, medical imaging equipment, autonomous robotics, intelligent transportation systems, etc. The computing elements like CPU, GPU, etc face issues like memory bandwidth, delay and power consumption due to increased resolution and frame rates. GPUs offer parallelism but have large power consumption and non-deterministic delay. The Field Programmable Gate Arrays (FPGAs) provide low power consumption, deterministic execution, reconfigurability, parallelism, etc along with extra capabilities of convolution structures, BRAMs, etc. As Sobel operator reduces noise by combining gradient computation with a smoothing effect using weighted kernels based on 3x3 masks to compute both horizontal and vertical gradients for parallel implementation on FPGA. However, it results in discontinuities, thick edges, poor localization, etc in noisy and variable lighting conditions.

The Canny operator provides low response, good localization, by using hysteresis thresholding for edge continuity, Gaussian smoothing to reduce noise, gradient magnitude and direction computation, and non-maximum suppression to thin edges. However, the multi-stage processing pipeline greatly increases latency, memory usage, and computational complexity. In FPGA-based edge detection systems, trade-off exists between detection precision and hardware efficiency. A hybrid Sobel-Canny operator based FPGA design uses pipelined and AXI protocol streaming to optimize real-time operation.This paper contributes hybrid Sobel–Canny FPGA architecture that combines low- complexity gradient estimation by using Sobel operator with high-precision edge localization by using Canny operator. This results in reduced computational complexity. The adaptive thresholding hardware implementation dynamically adjusts thresholds based on local image statistics to improve robustness under varying illumination conditions. The morphological operators remove spurious edges without requiring external post-processing by maintaining real-time throughput. The fully pipelined streaming FPGA design supports real-time video processing with minimal latency. Hence, the adaptive thresholding improves edge continuity in low contrast regions and noise suppression under illumination variation. Also morphological cleanup helps to remove isolated noise edges and broken edge fragments.

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II. LITERATURE SURVEY

[1] The VGG Net model extracts features, the side-edge output networks refine the rough edges produced by adaptive thresholding. For real time implementation, Xilinx ZYNQ- 7000 FPGA is used to implement Sobel edge detection algorithm along with to utilize parallel processing [2] on grayscale images. An automated star-counting for real time edge-detection and morphological feature extraction is presented for space surveillance in [3]. Other operators like Canny, Sobel, and Prewitt are assessed for varying intensity discontinuities. The modified Sobel method improves accuracy and processing performance with FPGA implementation is proposed in [4]. This method provides higher sensitivity and improved noise handling with faster edge recognition for better tumor contour detection in MRI images. To accomplish real-time image processing via FPGA, hardware implementation of the Sobel edge detection method is described in [5] For efficient gradient values, Sobel kernels are applied in both horizontal and vertical directions to improve throughput, reduce latency, and efficient resource utilization for combining picture acquisition and display modules. A bespoke Multiply–Accumulate (MAC) IP core of Xilinx Vivado design suite is used to speed up the Sobel edge detection technique is described in [6]. This MAC uses parallelism to reduce calculation time and latency. The FPGA implementation demonstrated increased speed, reduced energy consumption, and effective resource usage well suited for applications like autonomous navigation, object detection, video analysis, etc. A real-time FPGA based video edge detection with a resolution of 1280x720 at 30 frames per second is presented in [7]. This approach reduces processing times and improves edge quality by combining a median filter, Sobel operator, and morphological processes. A real- time Cyclone IV E FPGA based Sobel-based edge detection technique for detecting illnesses in Hevea (rubber tree) leaves is proposed in [8]. This system identifies three main diseases i.e., Colletotrichum Leaf Disease, Bird's Eye Leaf Spot, and Corynespora Leaf Spot. To overcome the inadequate edge localization, an enhanced Sobel operator for infrared image target extraction is suggested in [9] to better distinguish edge and non-edge pixels. Comparing experimental results to typical Sobel processing, better target extraction and greater localization are confirmed.An FPGA-based system that uses morphological image processing and inter-frame difference to recognize and track moving objects in real time [10] for real- time vision applications by achieving quick, effective object detection and tracking without a large computational cost. A real-time FPGA-based collision avoidance system is described in [11] that uses the Manhattan formula to estimate vehicle distance after processing camera video, converting frames to grayscale, and applying Sobel edge detection. The technology offers quick and accurate collision detection for autonomous vehicles by utilizing FPGA parallelism and low power to increase traffic safety. In order to accurately segment images and videos, edge detection is an essential pre- processing step in [12] by applying bilateral/gaussian noise filtering and CLAHE-based histogram equalization to enhance the Canny edge identification technique. An ARM- SoC and FPGA hybrid Canny edge detection system is proposed in [13]. Yocto Linux is run by the ARM core, and VGA display and image processing are handled by the FPGA. Avalon-ST Bridge IP cores facilitate communication. In [14], several threshold levels are introduced to solve the issue of excessive edge thickness encountered in prior techniques to generate more realistic edge representations and enhanced error management. An effective lane line detection method utilizing a Spatial Convolutional Neural Network (SCNN) in conjunction with Canny edge detection and the Hough Transform is shown in [15]. By capturing spatial correlations in road photos, SCNN enhances lane detection in challenging situations. While the Hough Transform accurately locates lane lines, cunning edge detection improves edge features. The integrated method works effectively in various road conditions and illumination conditions suitable for real- time autonomous driving and ADAS applications is demonstrated by experimental findings. An essential part of ADAS and autonomous driving applications is lane detection in [16] to increase accuracy in a variety of environmental circumstances like a lane detection method that combines Scharr-based Canny edge detection with the Hough Transform. With a low false positive rate of 2.1% and real- time performance at 28 ms per frame, the suggested technique achieves an average accuracy of 96.2%. A road lane detection and tracking system utilising Open CV with Gaussian Blur, masking, Canny edge detection, and the Hough Transform is shown in [17]. Real-time road footage at various times of the day were used to evaluate the system, which was constructed on an embedded controller with a vision sensor. An energy- efficient edge detection technique utilizing in-memory computation with SOT-MRAM is presented in [18] which reduces circuit complexity and power. A method for monitoring cutting tool defects is suggested in [19] for Flexible Manufacturing Systems (FMS) need great operational adaptability and little human intervention. Tool flaws can be precisely identified by size and location to vision- based non-contact inspection for enhanced reliability, real- time decision making and overall manufacturing system performance. The segmentation of underwater prawn images by using five edge detection techniques like Canny, Sobel, Prewitt, Roberts, and Laplacian of Gaussian (LoG) over a fog computing network are explored in [20] and evaluated to assess segmentation performance using PSNR and MSE measures.

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III. EXISTING ALGORITHM

The main goal of FPGA-based picture edge detection research has been to achieve real-time performance with constrained hardware resources. Because of their low computational complexity and appropriateness for parallel hardware realization, early implementations concentrated on straightforward gradient-based operators. To efficiently carry out convolution operations, these designs usually employ sliding window structures with line buffers.

Sobel-Based FPGA Edge Detection

Fixed 3x3 convolution kernels are used in Sobel-based FPGA systems to calculate both horizontal and vertical gradients. These systems are frequently able to process one pixel each clock cycle, making them extremely efficient in terms of logic consumption and processing speed. Compared to straightforward gradient operators, the Sobel operator is more resilient to noise since it also adds a slight smoothing effect. Nevertheless, Sobel-only implementations have a number of intrinsic drawbacks like only the horizontal and vertical directions can be used to compute gradients, as there are no suppression mechanisms, edge thickness is still high, Edge fragmentation results from fixed thresholding, Curved and diagonal edges are not well localized and the performance declines with changes in illumination.

Canny-Based FPGA Edge Detection

A number of researchers have used the Canny edge detection technique on FPGA devices to enhance edge quality. Gaussian filtering, gradient computation, non-maximum suppression, and double thresholding with hysteresis are some of the sequential processes that make up Canny-based designs. These designs greatly enhance edge continuity and localization. The FPGA implementations of Canny encounter significant obstacles despite their benefits like large convolution kernels and buffering are needed for Gaussian filtering, double thresholding raises latency and memory access, non-maximum suppression results in intricate control logic, frame-level buffering is frequently necessary and power usage and hardware costs rise sharply. Because of this, Canny- based FPGA designs frequently fall short of stringent real- time requirements, especially when dealing with high- resolution video feeds.

Hybrid and Optimized Approaches

By streamlining specific steps or integrating Sobel with partial Canny processing, some current studies try to lower Canny complexity. However, because of ineffective dataflow design, many of these methods result in increased latency, decreased scalability, or architectural complexity. Instead of utilizing their complementing strengths, the majority of current systems consider Sobel and Canny as separate modules.

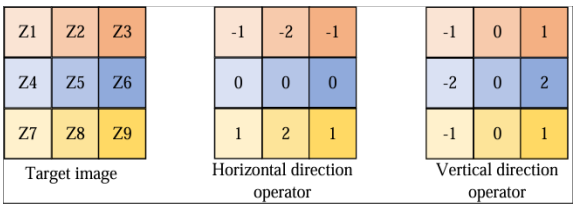

Fig.1. Traditional Sobel operator model

The Sobel operator's straightforward convolution structure and built-in smoothing feature in FPGA designs. By convolving the input image with two fixed 3x3 kernels that approximate first-order derivatives in both horizontal and vertical directions, it predicts image gradients.

Sobel Convolution Kernels

Suggested method is to achieve high edge detection accuracy with little latency and hardware complexity, which makes it appropriate for embedded vision applications that have stringent real-time and power requirements. The first step converts the input image into grayscale format, which is represented as I(x,y), where x and y stand for the spatial coordinates. The Sobel operator is initially used to extract coarse edge information because of its ease of use and compatibility with parallel hardware implementation. The Sobel operator uses horizontal and vertical 3x3 kernels to convolve the input image in order to calculate first-order intensity gradients. The gradient components that arise are Gx (x, y) and Gy (x, y) with variations in intensity in orthogonal axes (x, y). To reduce computational and resource complexity, the sum of absolute gradient components is used for gradient magnitude.

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$$\boldsymbol{Gx} = \begin{bmatrix} -1 & 0 & +1 \\ -2 & 0 & +2 \\ -1 & 0 & +1 \end{bmatrix}, \boldsymbol{Gy} = \begin{bmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ +1 & +2 & +1 \end{bmatrix} \quad (1)$$

For an input image (x,y), the gradient components are computed as:

$$(x, y) = (x, y) * Gx \quad (2)$$

$$(x, y) = (x, y) * Gy \quad (3)$$

Where * denotes convolution.
The gradient magnitude is then approximated as:

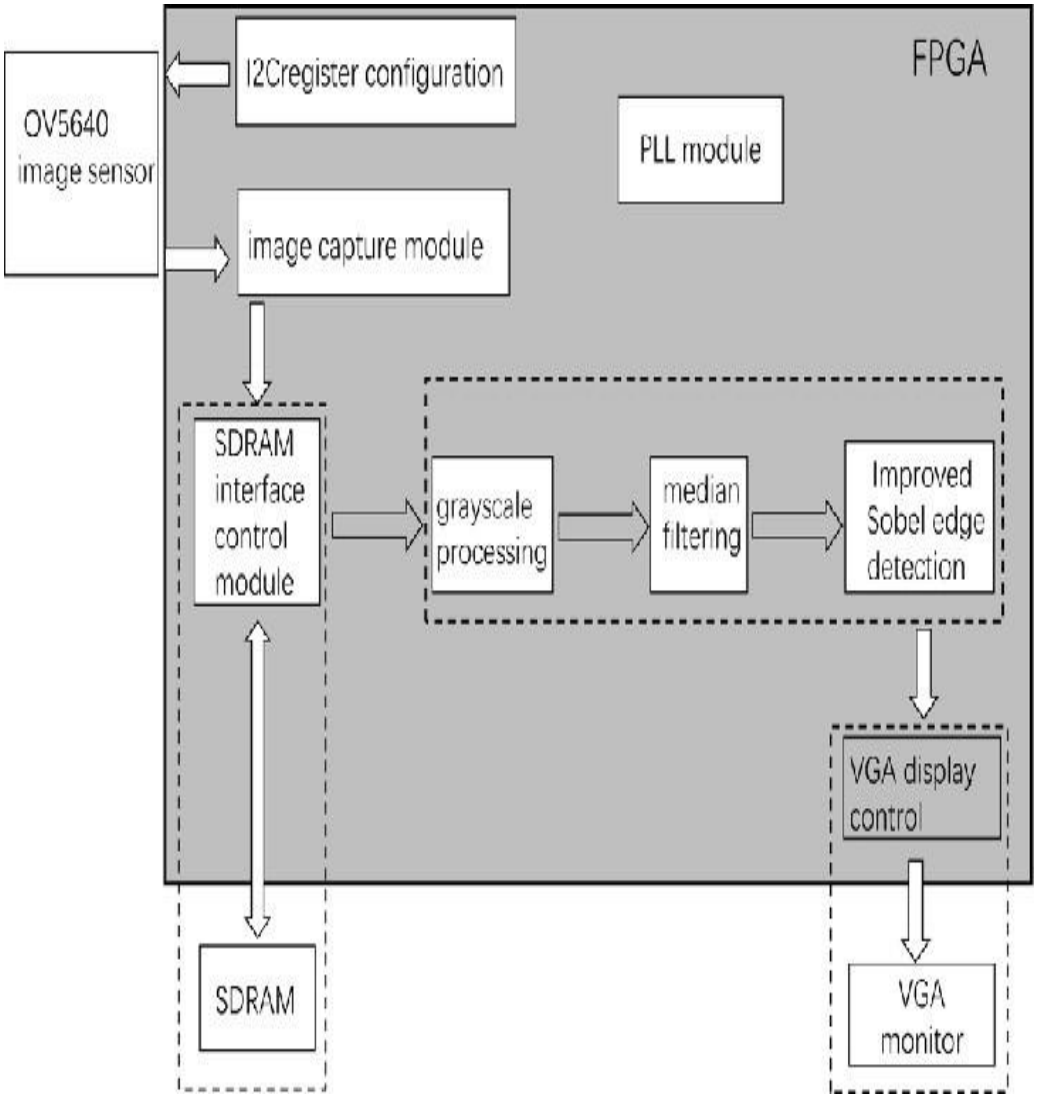

Fig.3. Proposed Architecture

The vertical to horizontal gradients ratio evaluates the gradient direction as a finite set of dominating orientations

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$(x, y) = 5G^2 + G^2 \text{or}(x, y) \approx | G$

$| + | G |$ (4)

after gradient computation to enable precise edge thinning

$x \quad y$

$x \quad y$

for the refining stage. The suggested architecture preserves the A pixel is classified as an edge if:

$(x, y) \geq T$ (5)

where $T$is a fixed threshold

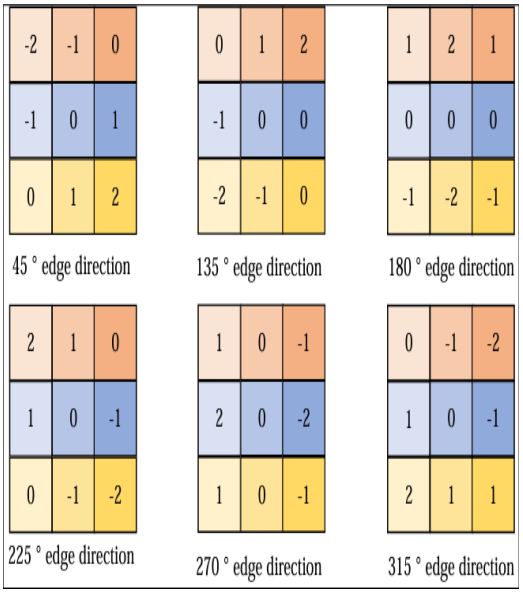

Fig.2. Improved Sobel operator model

But Sobel operator leads to fixed threshold T causes broken edges, no suppression - thick edges, poor diagonal edge localization, sensitive to illumination changes. The Canny edge detection presents a multi-stage optimization technique to get over Sobel constraints. FPGA implementation is difficult due to its computational complexity, despite its effectiveness.

IV. PROPOSED WORK

This work presents a hardware-efficient FPGA- based real-time edge detection architecture that combines Canny-based edge refining and Sobel-based gradient extraction into a single, pipelined processing framework. The Major goal of the fundamental directional properties of edges while streamlining control logic by limiting directional analysis to primary orientations. Gaussian smoothing is applied to the gradient magnitude image in order to reduce noise and enhance edge continuity. High-frequency noise components that could cause incorrect edge detection are reduced by the smoothing process. Two one-dimensional filtering operations can take the place of a complete two-dimensional convolution in the suggested design since Gaussian filtering is implemented using a separable convolution structure. This enhancement facilitates streaming and drastically lowers hardware resources usage. The non-maximum suppression is used after noise suppression to improve edge localization. Only local maxima are kept in this stage, where each pixel is compared to its neighboring pixels along the calculated gradient direction. This procedure produces thin, well- localized edges by removing thick and redundant edge replies generated by the Sobel operator. Because localized comparisons are used to implement the non-maximum suppression stage, pipelined FPGA execution is possible without the need for frame-level buffering.

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Mathematical Steps of Canny Edge Detection Include

(a) Gaussian Smoothing

$$G_\sigma(x,y) = \frac{1}{2\pi\sigma^2} \exp\left(1 - \frac{x^2+y^2}{2\sigma^2}\right) \quad (6)$$

V. RESULTS AND DISCUSSION

These operations use Verilog HDL Modeling and are evaluated for Zynq 7000 series FPGA (XC7Z020-1CLG484). The smoothed image is:

$$(x,y) = (x,y) * G_\sigma(x,y) \quad (7)$$

(b) Gradient Computation

The images are verified in MATLAB. The basic and improved pipelined architecture uses adaptive thresholding and morphological cleanup as additives yield the results of image with size 532 x 800, number of pixels as 425600, sigma as 1 are as shown in fig.4, where the improved pipelined operations provide better results when compared to basic version.

$$G_x = \frac{\partial}{\partial x}, G_y = \frac{\partial I_S}{\partial y} \quad (8)$$

$$(x,y) = 5\sqrt{G^2 + G^2} \quad (9)$$

$$(x,y) = \tan^{-1}\left(\frac{G_y}{G_x}\right) \quad (10)$$

(c) Non-Maximum Suppression

A pixel $(x, y)$is retained as an edge only if:

$$(x,y) = \max\{M \text{ along gradient direction}\} \quad (11)$$

This produces **thin edges**, but requires neighborhood comparison and directional logic.

(d) Double Thresholding & Hysteresis

Strong edge, $M \geq T_H$

Basic Pipelined operations

(x,y) = I Weak edge, $T_L \leq M < T_H$

Non-edge, $M < T_L$

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(12)ImprovedPipelinedoperations:

Fig.4. Results of input and output images

Weak edges are preserved only if connected to strong edges.
Double thresholding is then used to classify pixels in the revised gradient image into three categories: strong edges, weak edges, and non-edge pixels. While a lower threshold permits the retention of prospective edge pixels for additional analysis, a high threshold identifies edge pixels that are confident. An edge tracking via hysteresis method, which preserves weak edges only if they are related to strong edges within a small neighborhood, is used to guarantee edge continuity. This process preserves continuous edge structures while efficiently eliminating isolated noise responses. Pixel- level processing at every clock cycle is made possible by the implementation of the complete edge detection pipeline as a fully streaming and pipelined design. Sliding windows for convolution operations are created using line buffers, which greatly reduces latency and does away with the requirement for entire image storage. The suggested design strikes a fair compromise between hardware efficiency and detection accuracy by fusing the superior localization and refinement stages of the Canny algorithm with the low-cost gradient extraction capacity of the Sobel operator. The suggested method is ideal for contemporary embedded vision systems that need precise, low-latency edge detection.

The image based statistics are as shown in table I. The sobel_T_norm reflects sensitivity of Sobel detector and signifies how strong a gradient must be to be considered an edge in Sobel. The canny_T_norm indicates robustness of Canny to noise vs. detail preservation and the hysteresis limits of canny. The canny_T_norm indicates robustness of Canny to noise vs. detail preservation and the hysteresis limits of canny. The canny_T_hw_approx shows implementation loss between ideal software Canny and FPGA/ASIC version. The N_sobel, N_canny signify the total amount of structure each algorithm detects. N_final represents usable edges for next stages (object detection, segmentation). The density_sobel, density_canny and density_final are used as objective quality indicator. The mean_mag signifies average edge strength or overall contrast level in image. The std_mag signifies the variation of edge strengths and indicates dynamic range of details. The max_mag relates to global contrast peak, signifies strongest edge present and is used to normalize thresholds. The dir_bins signifies angular resolution used to study orientation and determines how finely we analyze edge directions. The dir_hist signifies distribution of edge orientations and used for texture classification, HOG features and checking detector bias.

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TABLE I. COMPARSION TABLE FOR IMAGE BASED STATISTICS.

Parameter	Basic Pipelined Operations	Improved Pipelined Operation
sobel_T_norm	0.1569	0.1747
canny_T_norm	[0.0813 0.2031]	[0.2186 0.4677]
canny_T_hw_approx	[21 52]	[56 119]
N_sobel	138255	127680
N_canny	53266	33739
N_final	48351	49338
density_sobel	0.3248	0.3000
density_canny	0.1252	0.0793
density_final	0.1136	0.1159
mean_mag	1.2632	1.2761
std_mag	0.6135	0.5905
max_mag	2.5673	2.5671
dir_bins	[-180 -150 -120 -90 -60 -30 0 30 60 90 120 150 180]	[-180 -150 -120 -90 -60 -30 0 30 60 90 120 150 180]
dir_hist	[3569 3898 4813 4003 3701 4348 3506 3929 4781 3998 3521 4284]	[3860 3548 4552 3662 3679 5341 4003 3598 4361 3824 3590 5320]

When compared with basic pipelined operations, the improved pipelined operations improve by 10.18%, 62.8% and 56.57%, 62.5% and 56.3%, 7.6%, 36.6%, 2%, 7.6%,36.6%, 1.98%, 1.01% and 3.74%, for sobel_T_norm, canny_T_norm, canny_T_hw_approx, N_sobel, N_canny, N_final, density_sobel, density_canny, density_final, mean_mag and std_mag respectively. The max_mg and dir_bins are almost similar for both but dir_hist shows improvement.

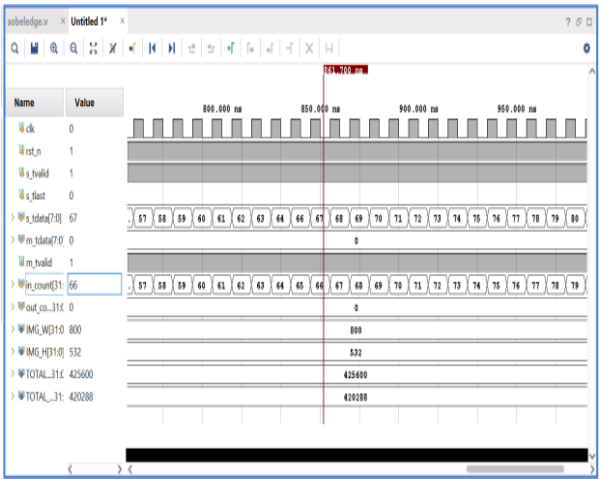

Fig.5.Simulation Results for Hardware

The simulation waveform is shown in fig.5, where the the output in the text file changes for every clock cycle. The hardware based statistics are evaluated in table II. When compared with basic pipelined operations, the improved pipelined operations improve the parameters by 48.69%, 46.11%, 50%, 32.66%, 5.7%, 39%, 54.74%, 51.75%, 40.16% and 48.97% for slice LUTs, logic LUTs, memory LUTs, slice registers, setup time, hold time, total power dissipation, logic power, signal power, dynamic power and number of cells respectively. The extracted implementation schematics are as shown in fig.6.

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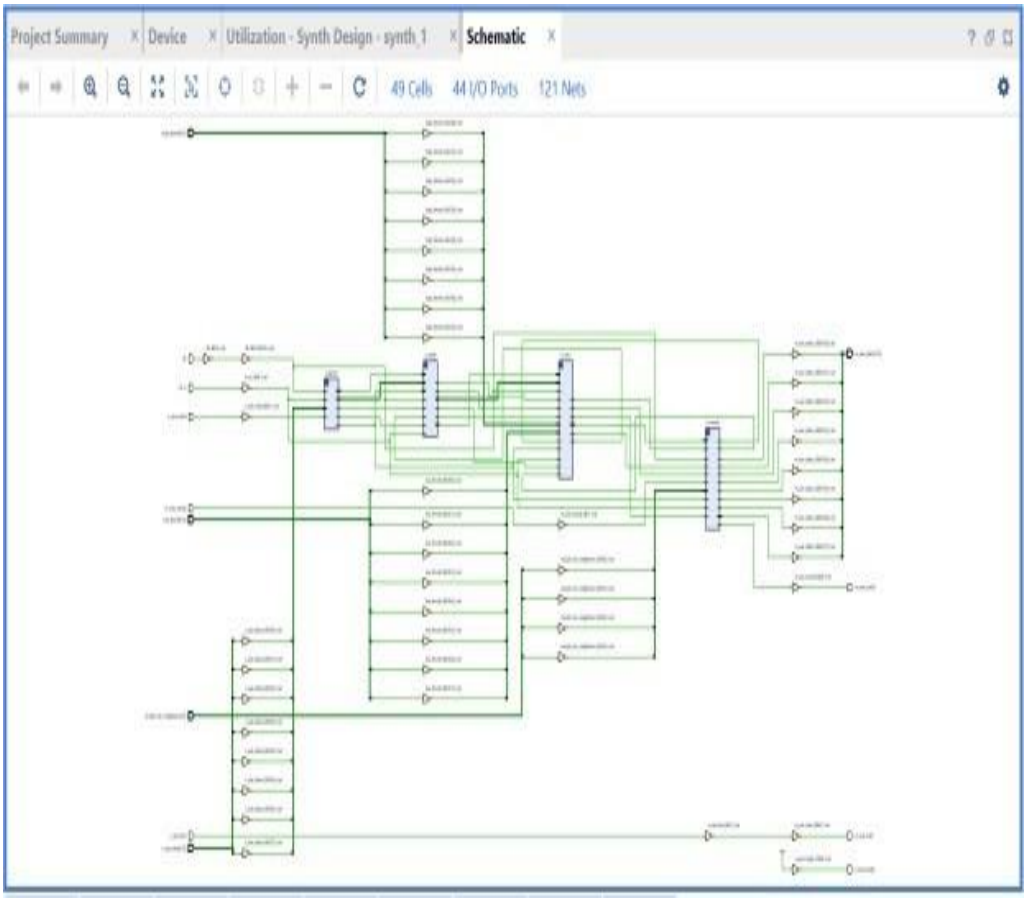
TABLE.II. COMPARSION TABLE FOR HARDWARE BASED STATISTICS

Parameters	Basic Pipelined Operations	Improved pipelined Operations
#Slice LUTs (out of 53200)	1879	964
LUTs as Logic	631	340
LUTs as Memory (Out of 17400)	1248	624
Slice Registers (Out of 106400)	251	169
tsetup (ns)	14.594	13.761
thold (ns)	0.288	0.289



Pipelined Operations

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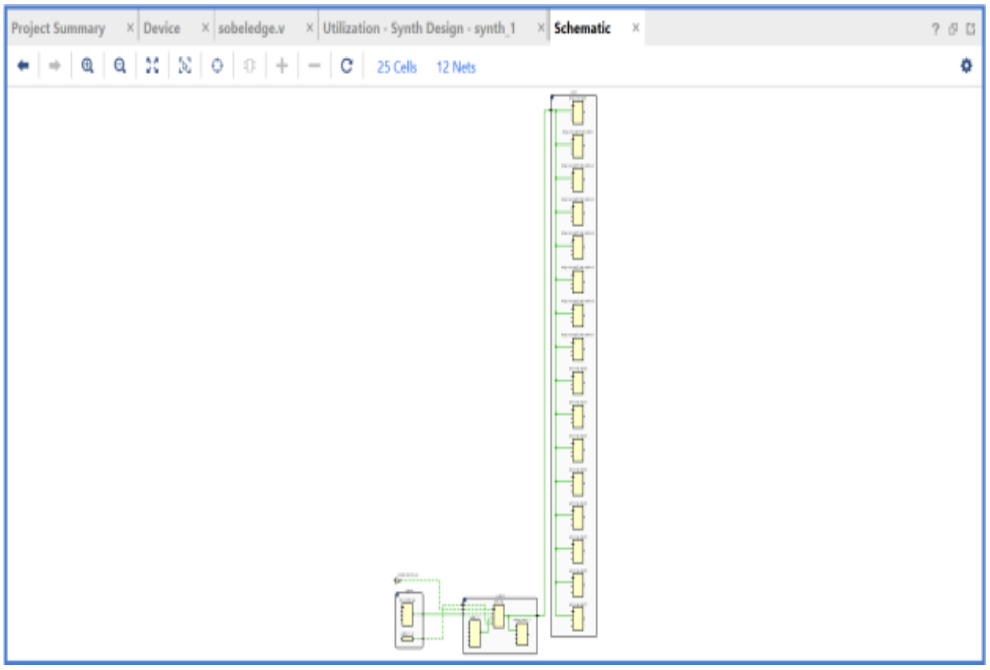

Improved Pipelined Operations

Fig.6.Implementation schematic for hardware

The state of art comparison with existing designs is as shown in table III with respect to latency and resource usage. The improvements are observed as 1.46% to 26.8% and 49.02% to 50.2% respectively.

TABLE.III. COMPARSION TABLE WITH EXISTING WORKS

Work	Latency	Resource Usage
[2]	8.303ns	1938 LUTs
[6]	6.161 ns	1908 LUTs
[13]	6.380ns	1901 LUTs
Proposed Method	6.071ns	964 LUTs

These results are scalable to 720p, 1080p, 4K, etc with strategies like multi-bank BRAM buffering, parallel pipeline duplication and AXI burst optimization. However, the bottlenecks can be requirement of external memory bandwidth and control synchronization at higher frame rates.

VI. CONCLUSION

The image edge detection is carried out using Sobel and Canny operator pipeline with improvement as adaptive thresholding and morphological cleanup is devised. The smoothing effect is provided by Sobel operator and good

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accuracy is provided by Canny operator to produce sharper and cleaner edges by applying gaussian smoothing. This efficient pipelined architecture provides a fully pipelined, streaming hardware approach, enabling continuous pixel-level processing with minimal latency for real-time image edge detection. The designs use Zynq 7000 Series FPGA based on Verilog HDL for implementation. The simulation results confirm that the combination of Sobel's low-cost gradient extraction with Canny's superior edge refinement provides 5.7% to 62.5%. In future, the designs can be extended to other morphological operators.

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